CMOS SCALING BEYOND 10 nm
AND ENABLEMENT THROUGH 450 MM INFRASTRUCTURE

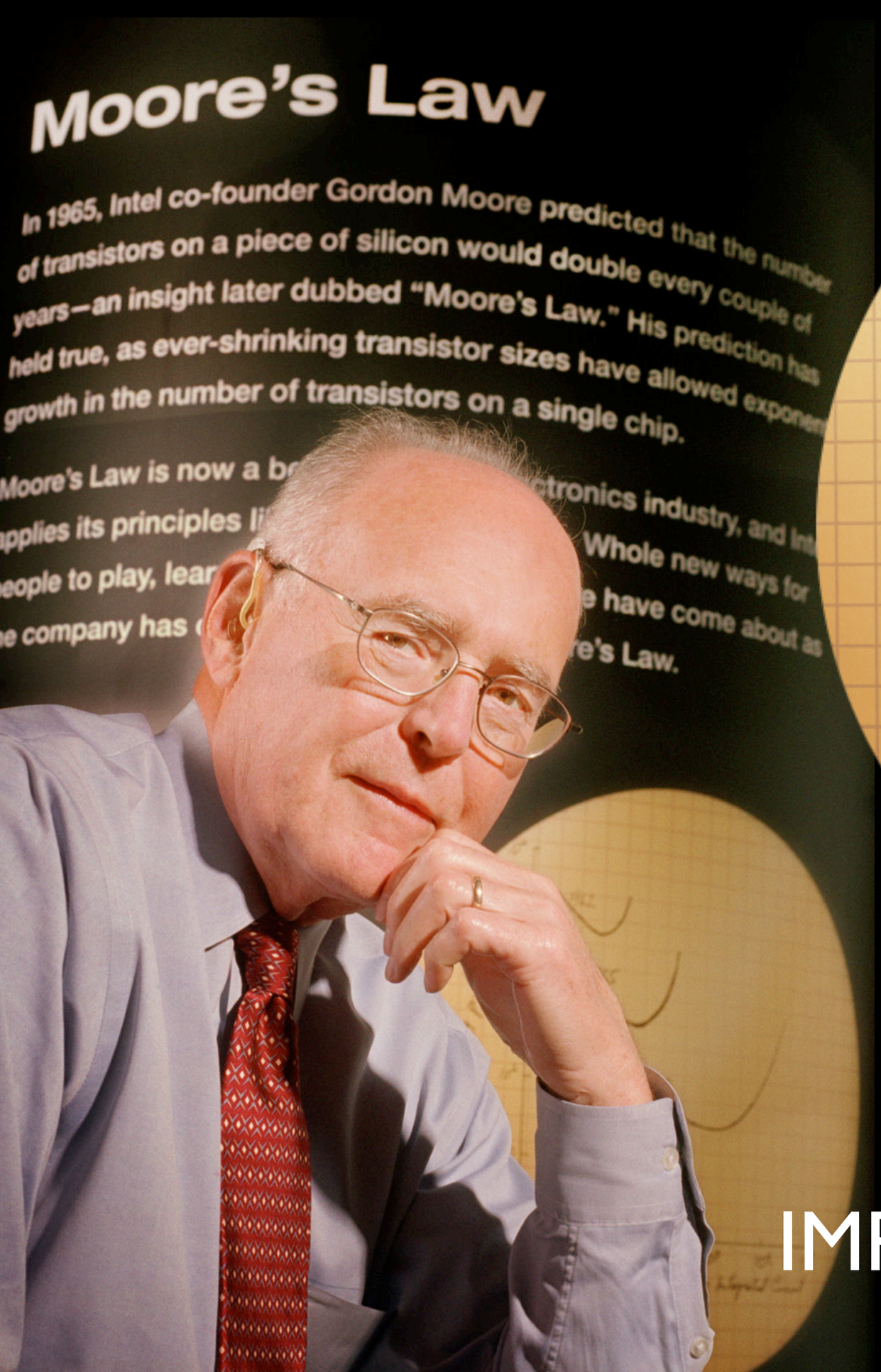
LODE LAUWERS
VICE PRESIDENT, PHD
CMOS BUSINESS DEVELOPMENT

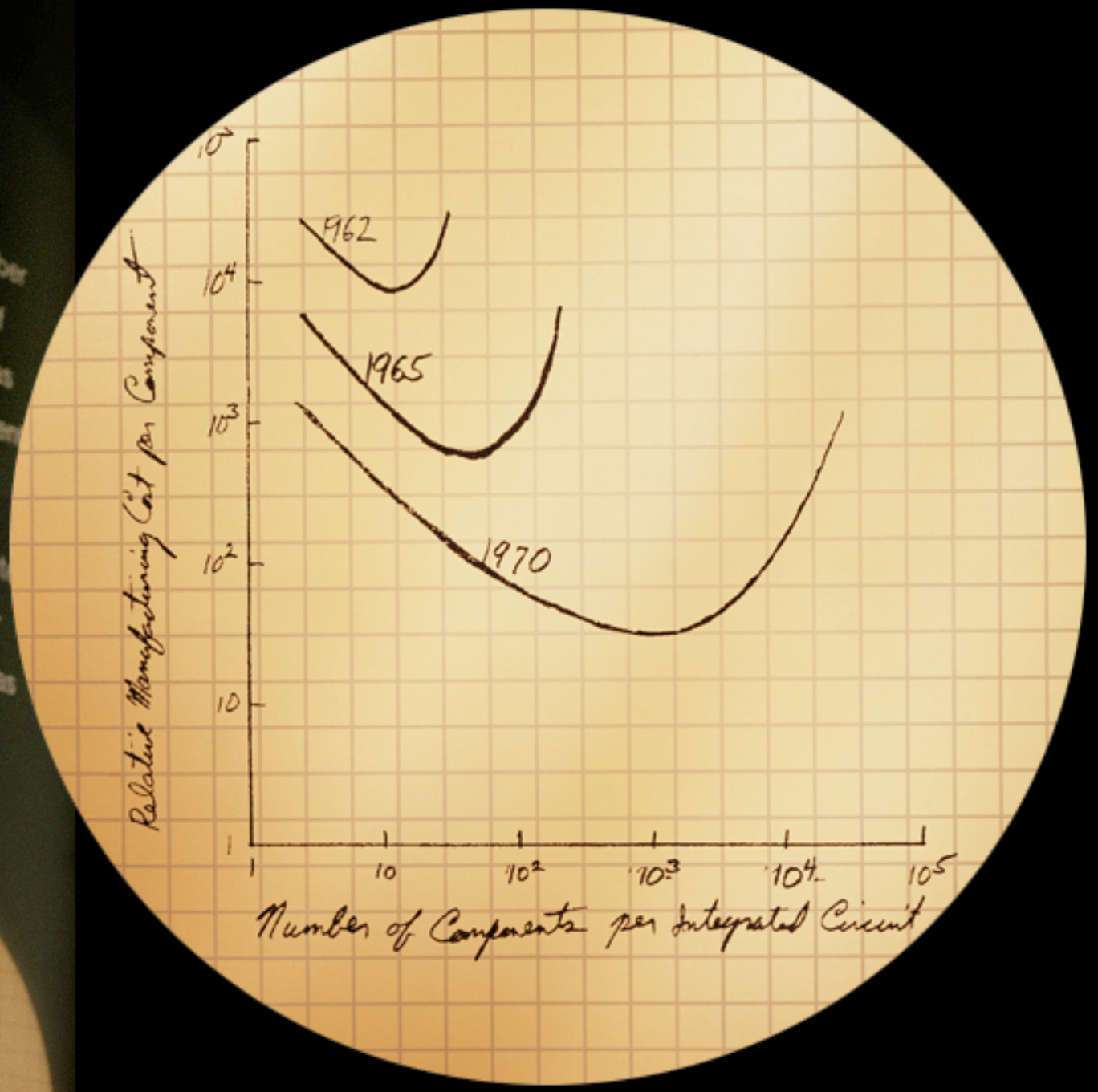
JUNE 2013

Moore's Law

In 1965, Intel co-founder Gordon Moore predicted that the number of transistors on a piece of silicon would double every couple of years—an insight later dubbed "Moore's Law." His prediction has held true, as ever-shrinking transistor sizes have allowed exponent growth in the number of transistors on a single chip.

Moore's Law is now a b ctronics industry, and int applies its principles li Whole new ways for eople to play, lear e have come about as e company has e's Law.





COST SCALING

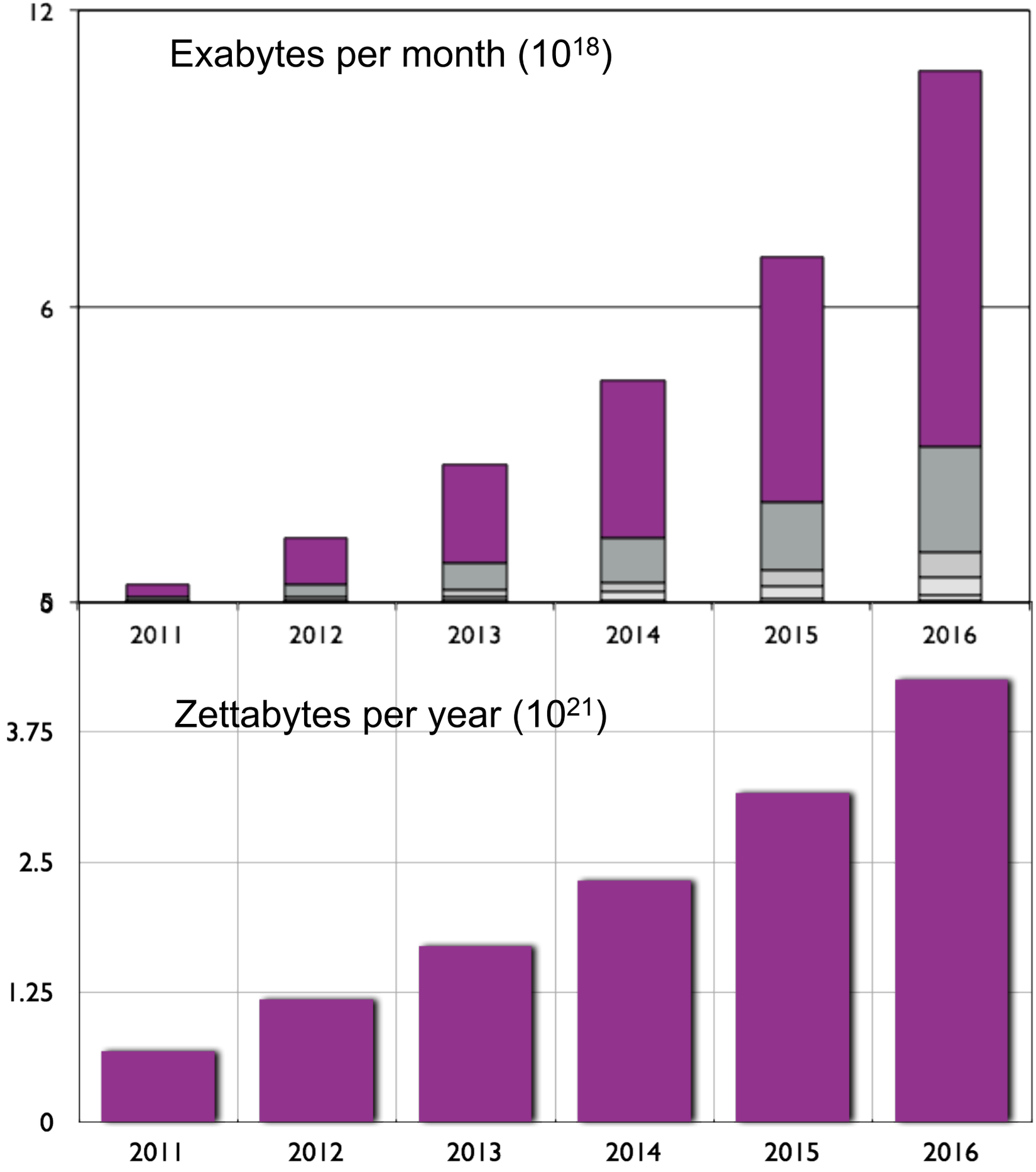
IMPROVED PERFORMANCE

MOBILE COMMUNICATION & COMPUTING DRIVING US FORWARD

GLOBAL TRAFFIC FORECAST

MOBILE DATA

Exabytes per month (10^{18})



CLOUD TRAFFIC

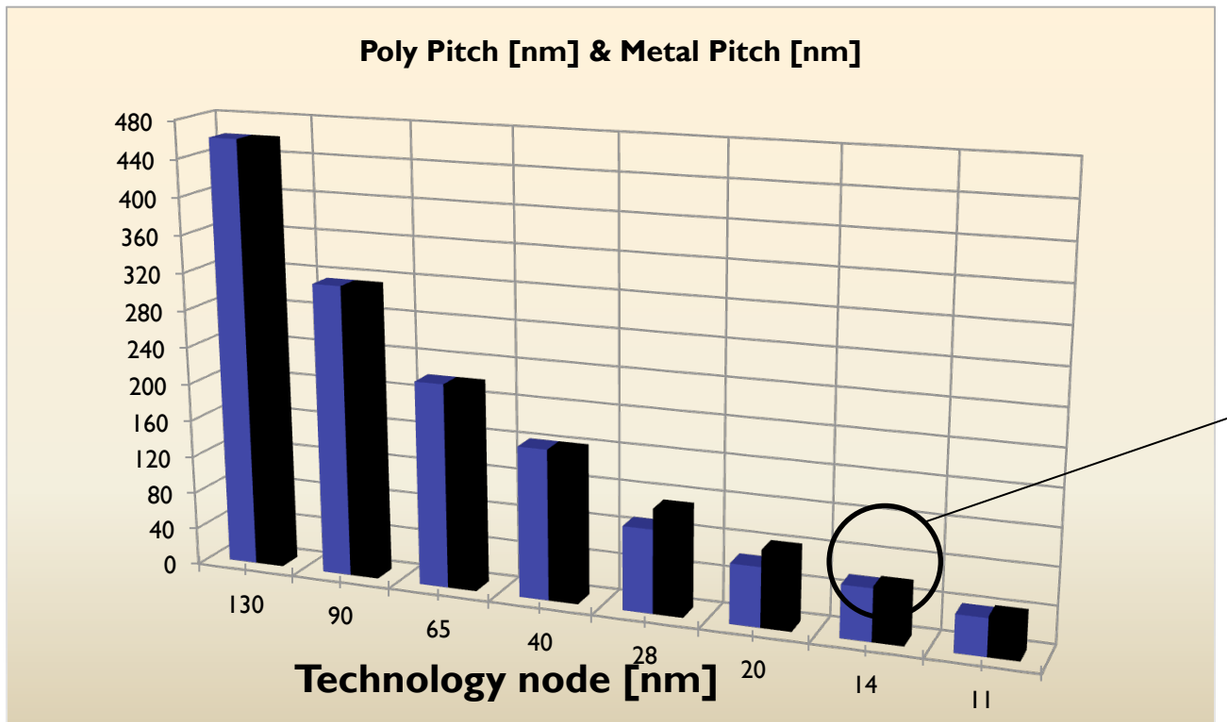
Zettabytes per year (10^{21})

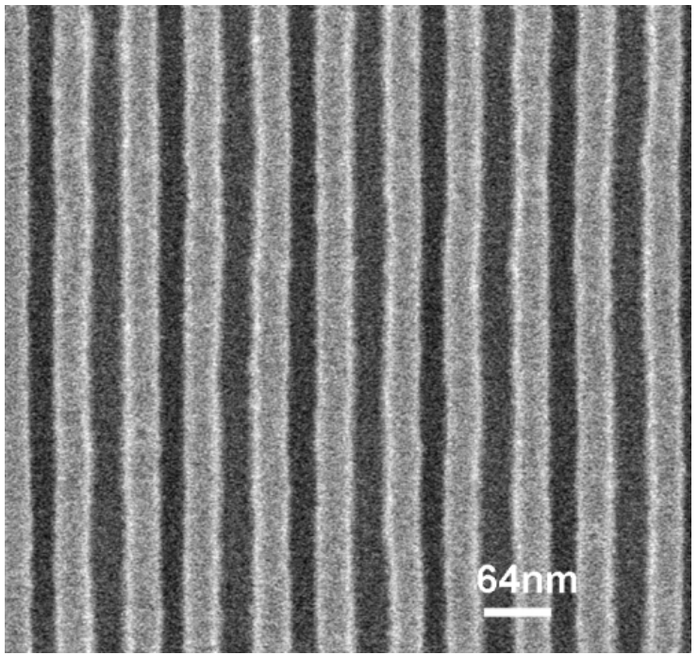
February 2012, Cisco VNI Global Mobile Data Traffic Forecast, 2011 - 2016

unprecedented

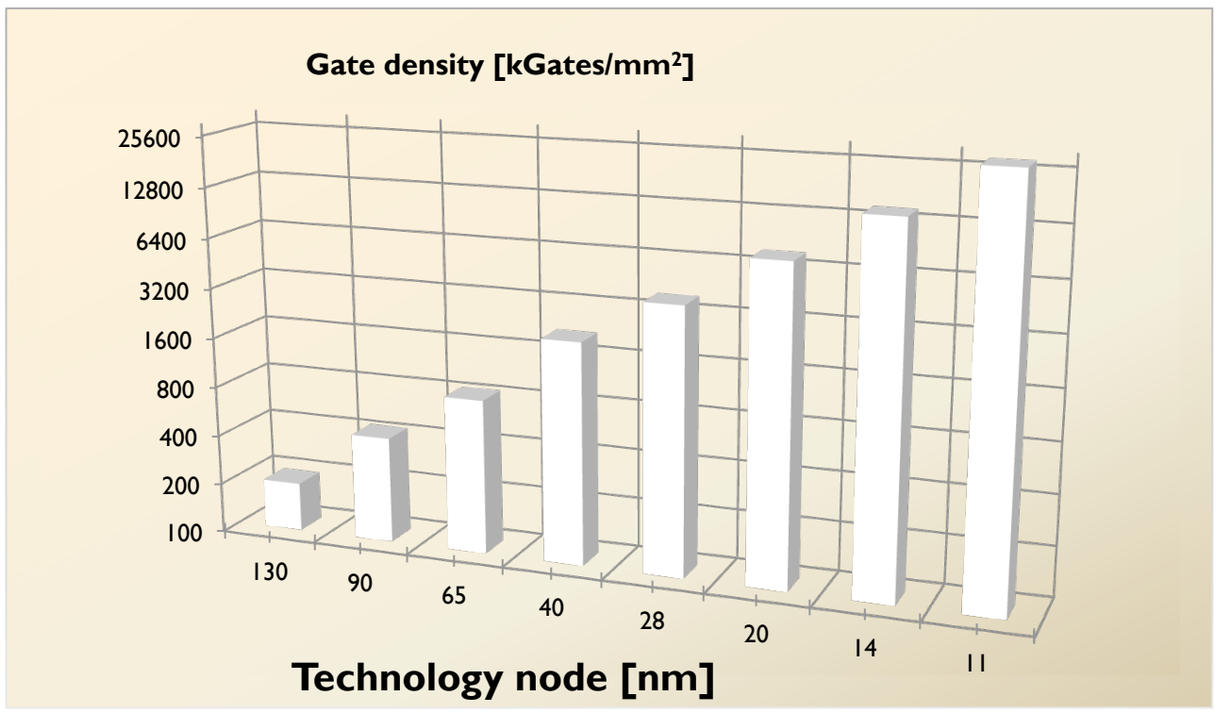
OPPORTUNITIES

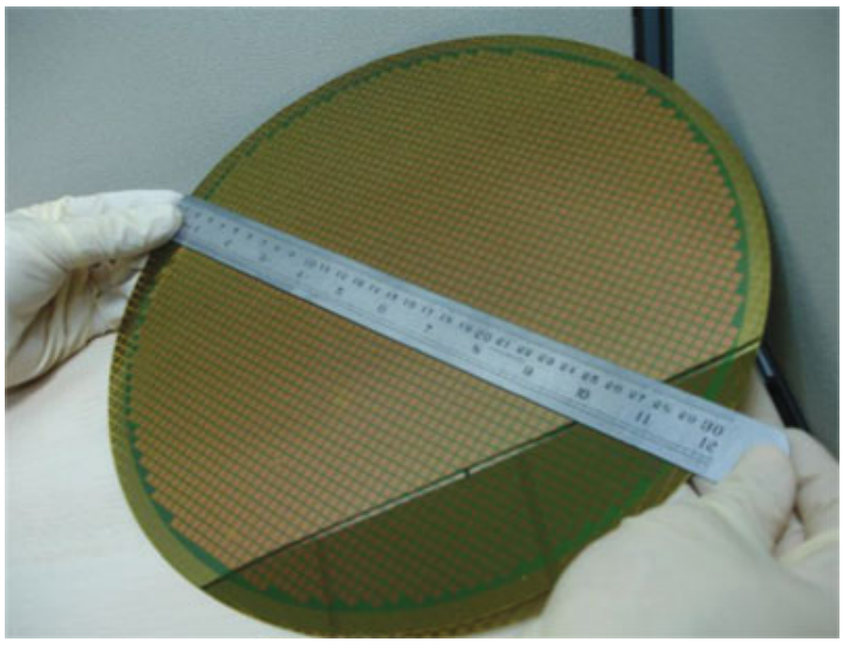
Increasing # transistors / area





Poly patterning at 64nm pitch





Increased gate density brings low-cost, low-power, high-performance

INCREASING TECHNOLOGY COMPLEXITY

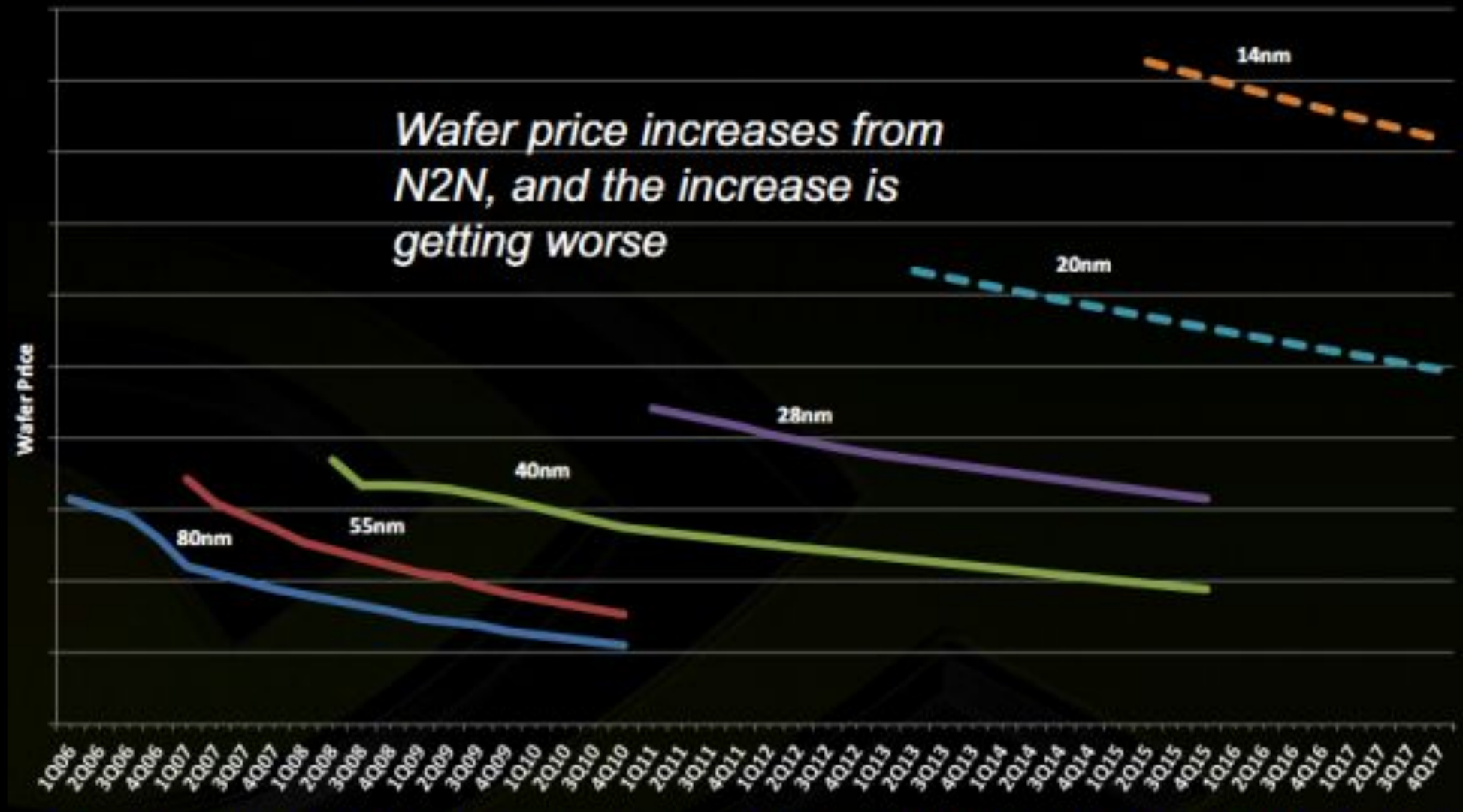
Scaling down to <10nm

EUV Litho
Multi pat.
HKMG
FDSOI
FinFET
Ge / IIIV
TFET
Nanowire
STT-MRAM
RRAM
3D SONOS
.....

‘60 **‘70** **‘80** **‘90** **‘00** **‘10**

© IMEC 2013

Wafer price is hiking up



- *The wafer price increase washes away the scaling benefit -> little saving in X'tor cost…need to lower CoO, simplify process, better yield...etc.. to incentivize Fab customers to 20 and 14nm.*
- *Collaborate to move to bigger (450mm) wafers*

unprecedented
CHALLENGES

3D NAND

AIRGAPS

PHOTONICS

FeRAM

DSA

SADP

3D VRRAM

TFET

3D INTERPOSER

FINFET

FDSOI

GE FINFET

STTRAM

RERAM

PCM

IIIV FINFET

3D TSV

LELE

ITIMTJ

3D-SONOS

GRAPHENE

EUV

OPTICAL IO

NANOWIRES

QUAD PATTERNING

CNT

QBITS

PCRAM

SPINLOGIC

Imec technology roadmaps

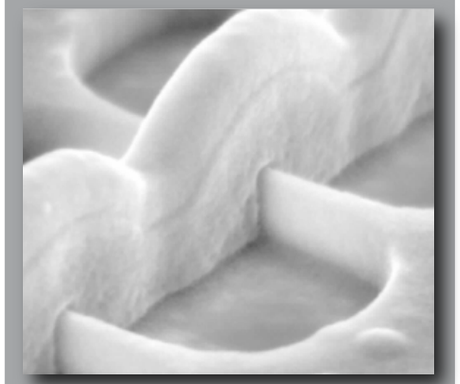
DEVICE SCALING

MATERIAL DEVICE MATERIAL DEVICE MATERIAL

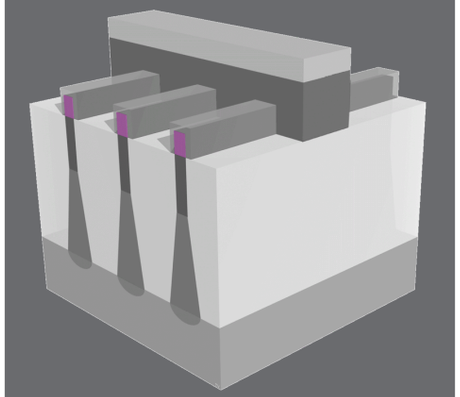
METAL GATE HIGH K



FINFET



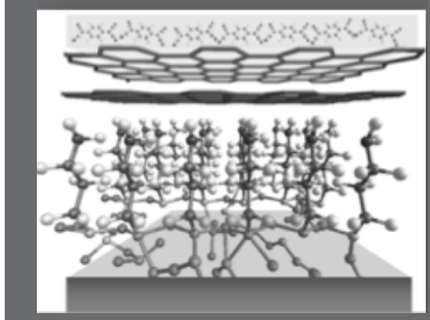
HIGH MOBILITY CHANNELS



NANOWIRE/ TUNNEL FETs



2D MATERIALS



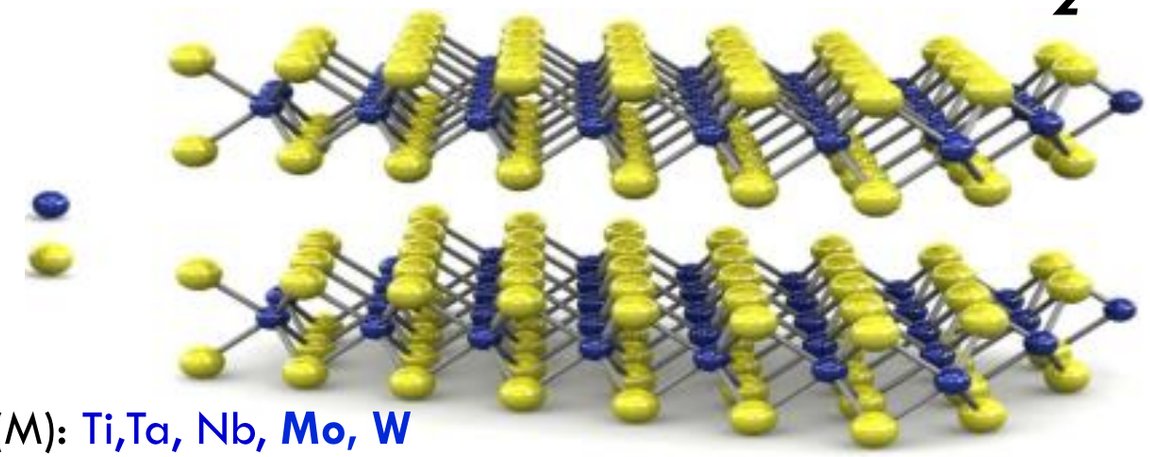
45nm | 32/38nm | 22/20nm | 14nm | 10nm | 7nm | 5nm | ...

Tech Node

IMEC's CMOS program is further exploring the limits of system scaling. With Leading industry partners, IMEC is investigating the challenges to realize platforms for the N10 and N7 node, and beyond.

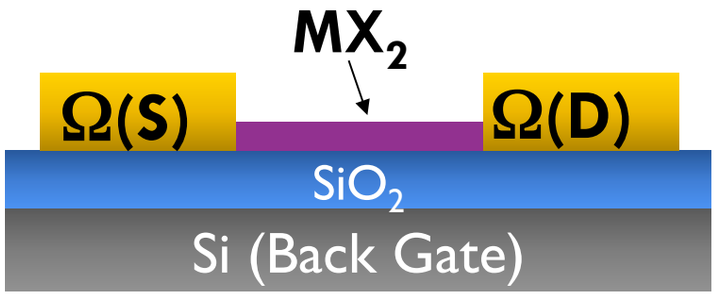
2D MATERIALS HIGHLIGHT: MOS_2 NFET & WSE_2 PFET

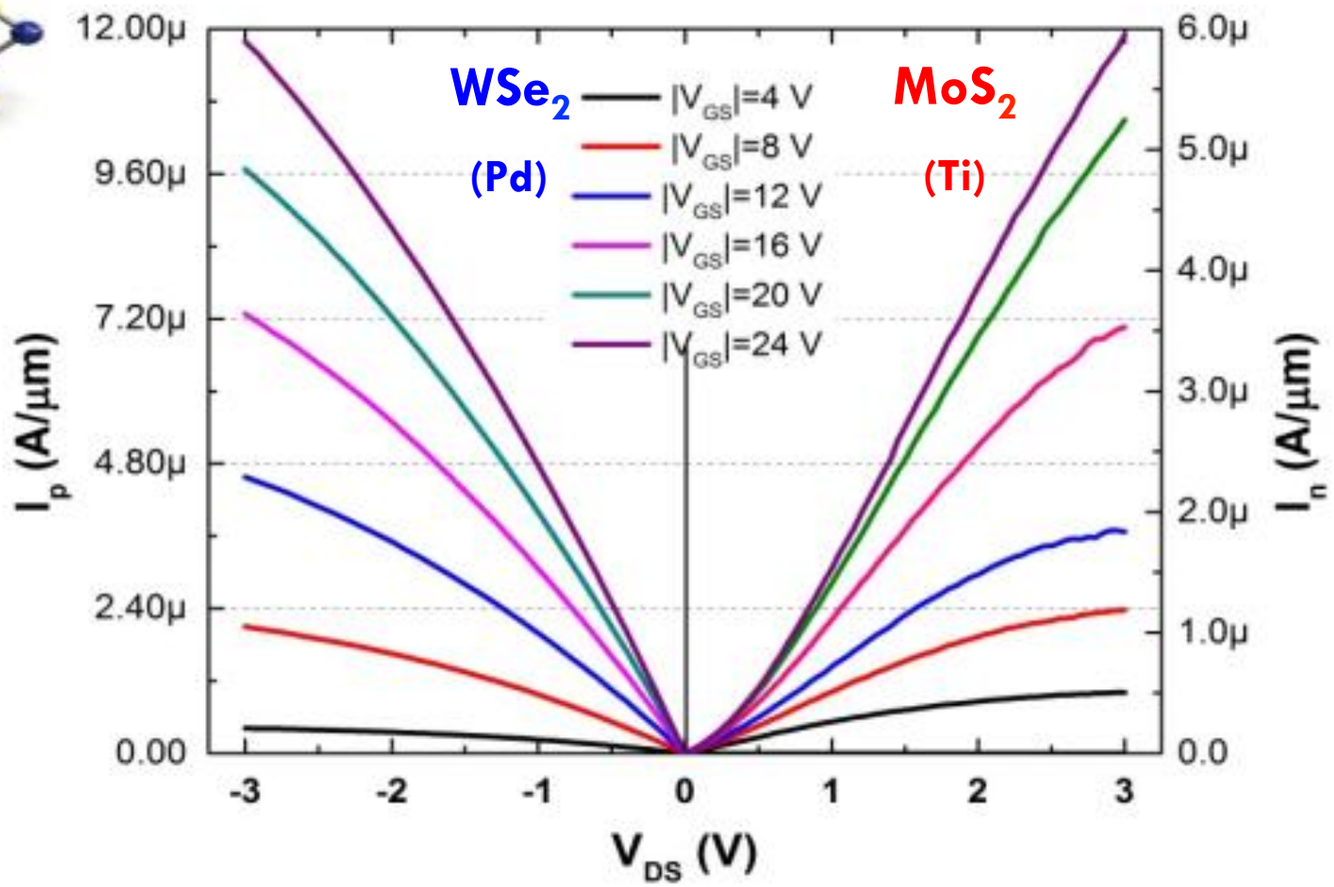
Common formula: MX_2

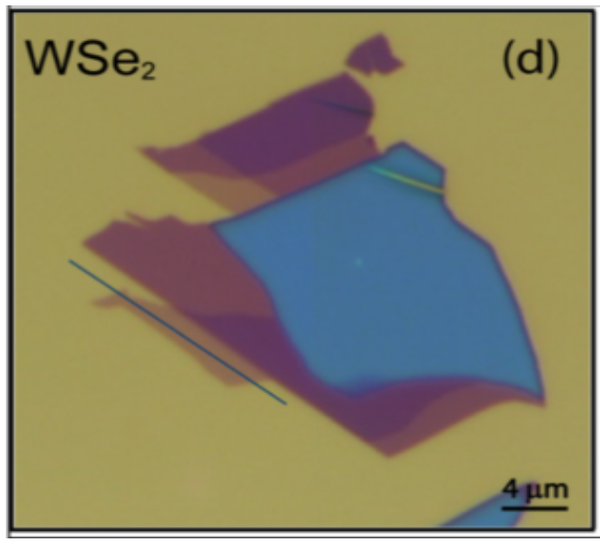


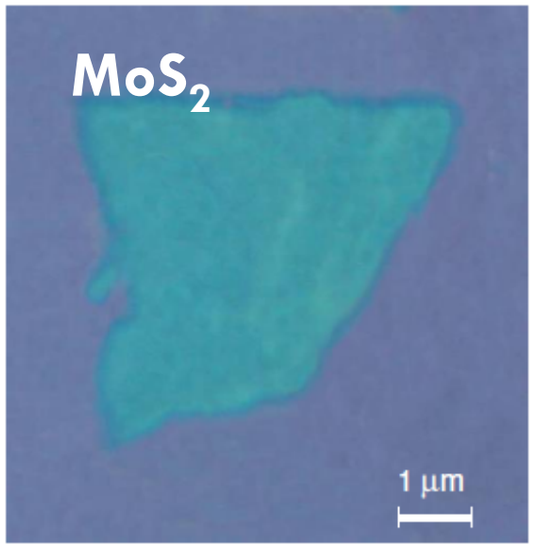
Metal (M): Ti,Ta, Nb, **Mo, W**

Chalcogenide (X): **S, Se**, Te





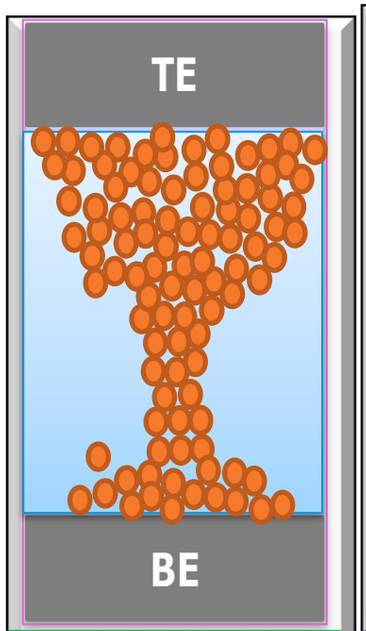
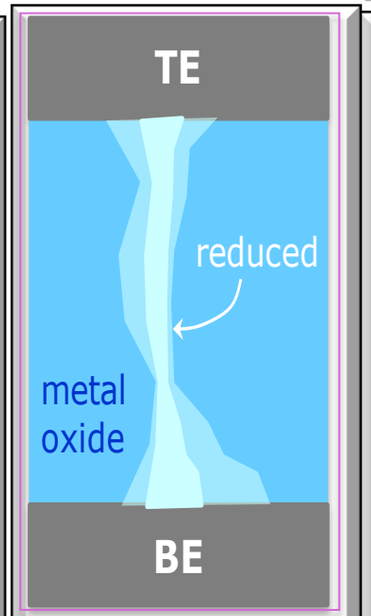
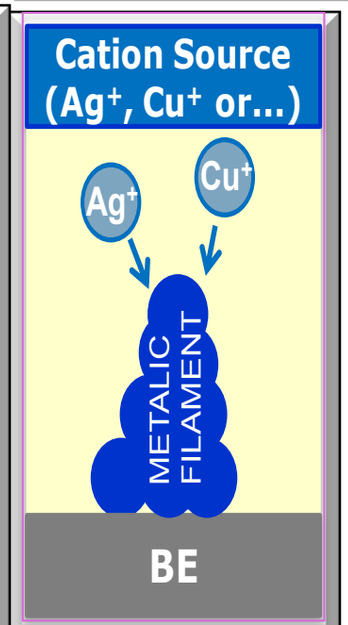
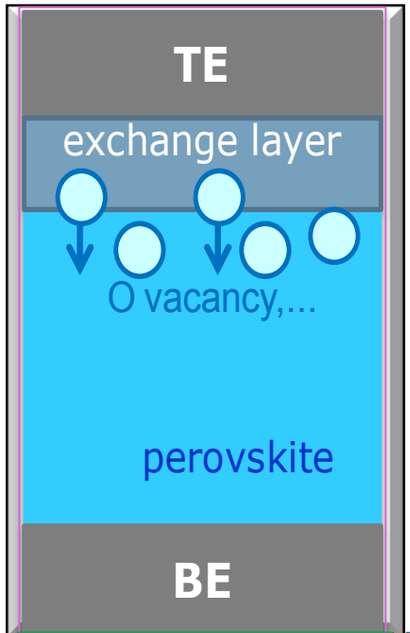
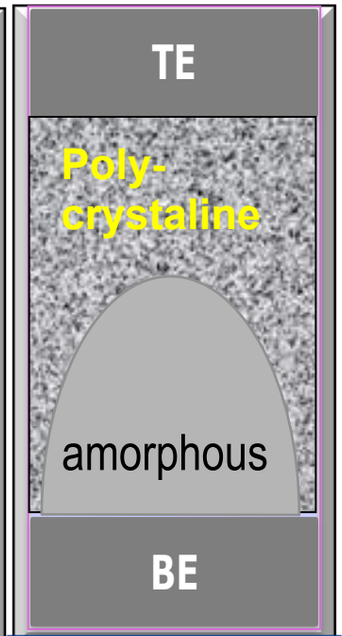
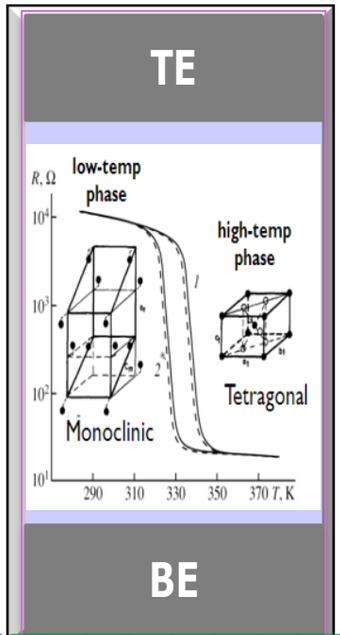
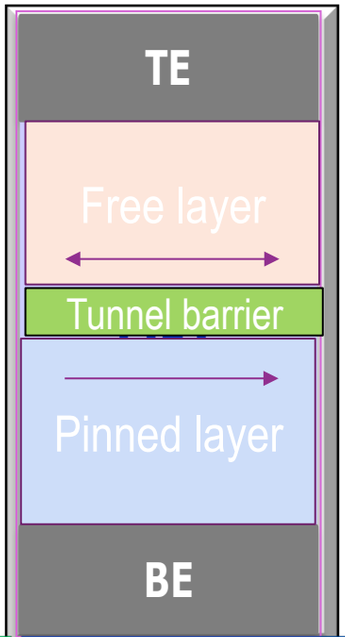




- 2D transitional metal/dichalcogenides: Demonstrated electrical devices with Molybdenum disulfide (MoS_2) nFET & Tungsten diselenide (WSe_2) pFET
- Work on-going to study the doping, contacting and transport of such materials

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EMERGING MEMORY:
RESISTIVE RAM - MATERIAL SYSTEMS

1D Filamentary			2D Interfacial	3D Bulk Transition			
Oxygen vacancy migration	Thermo-Chemical Fuse/ antifuse	Electro-chemical	Schottky barrier	Phase change	Electronic MIT	Tunnel Magneto resistance	
							
BIPOLAR	UNIPOLAR	BIPOLAR	BIPOLAR	UNIPOLAR	BIPOLAR	UNIPOLAR	
HfO_x $HfAlO_x$ HfO/AlO TaO_x		Cu/TiW/ AlO	AlO/TiO_x AlO/TaO_x		VO_2 $SmNiO_3$		

STT-MRAM : NOVEL MATERIALS, SIGNIFICANT INFRASTRUCTURE CHALLENGE



ANELVA PVD/RTA cluster



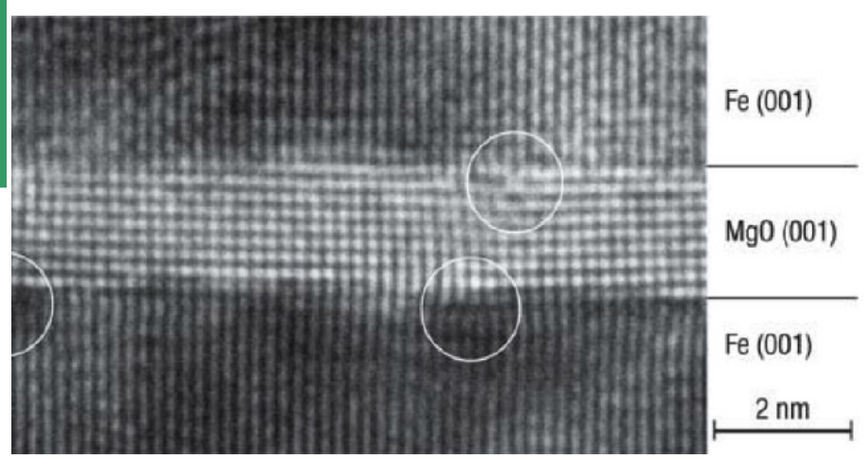
TEL etch/encapsulation cluster



Kerr Mapper



CIPT

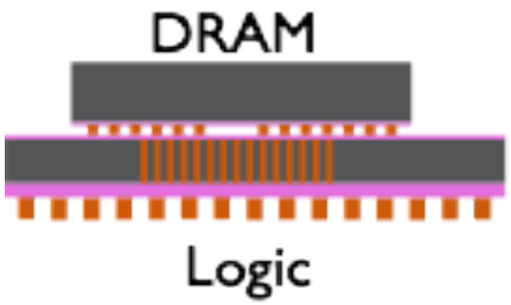


BKM p-MTJ
Ru 70Å
Ta 100Å
Co 4.5Å
[2.5ÅCo/8ÅPd] x 13
Pd 8Å
Co 4.5Å
Ru 8.5Å
Co 4.5Å
[2.5ÅCo/8ÅPd] x 3
Pt 10Å
Co 10Å
Ta 6Å
$Co_{24}Fe_{56}B_{20}$ 13Å
MgO x
$Co_{24}Fe_{56}B_{20}$ 11Å
Ta based BE

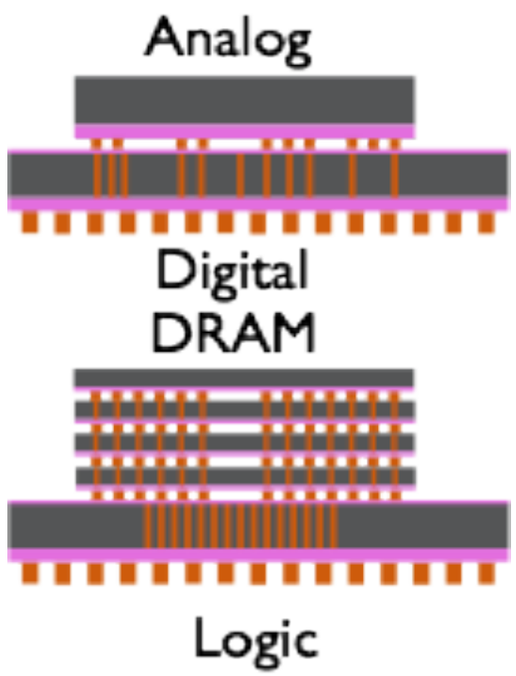
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3D enabled SCALING

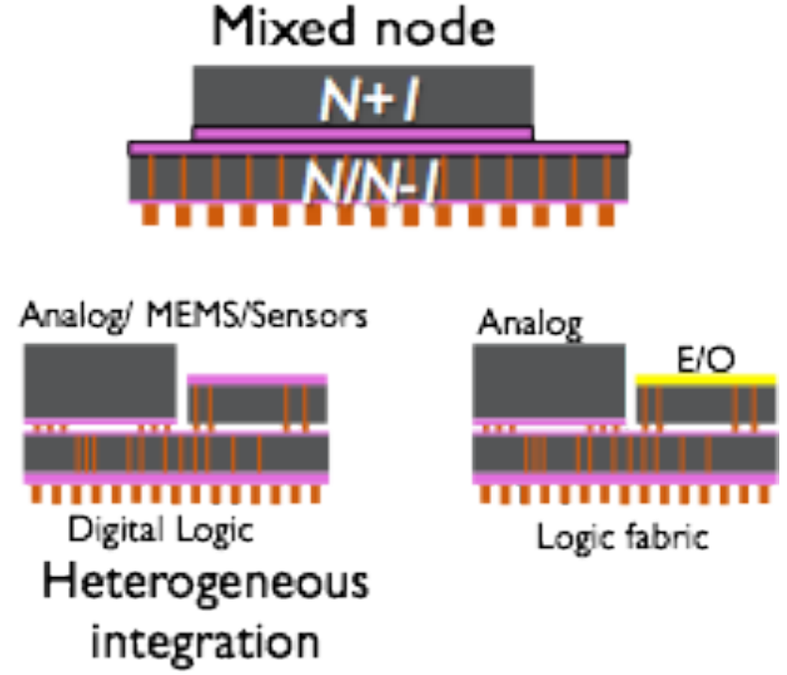
Gen.1
2012 - 2013



Gen.2
2014 - 2015



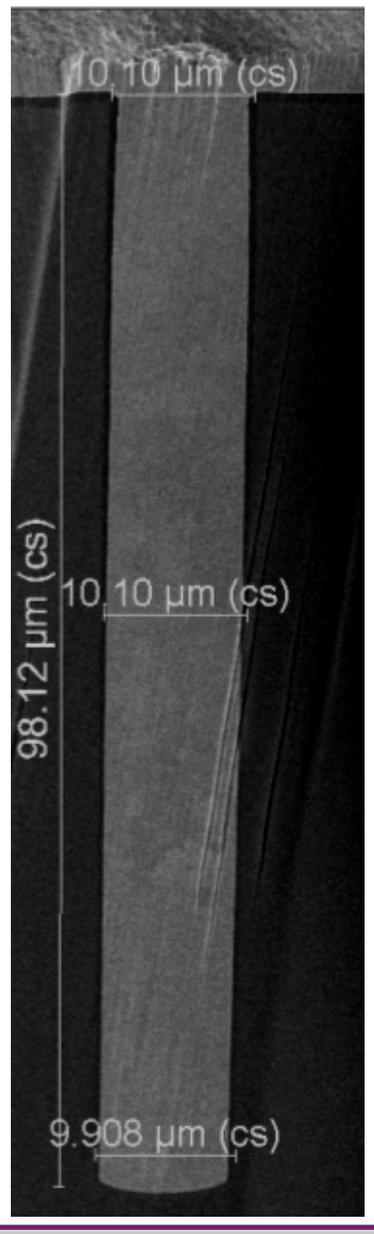
Gen.3
2016 - ...



3D- TSV SCALING ROADMAP

Reverse scaling for interposer applications

10µm Ø,
100µm deep,
AR 10:1

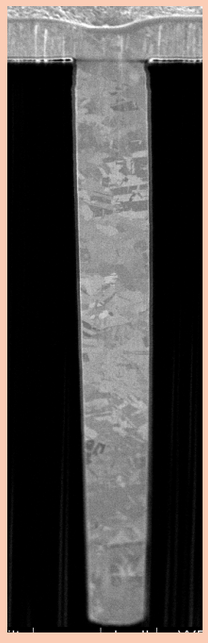


2012-13 ←

Ø ↗↗
AR ≡
Depth ↗↗

POR TSV Today

5µm Ø,
50µm deep
AR 10:1



2013-14 →

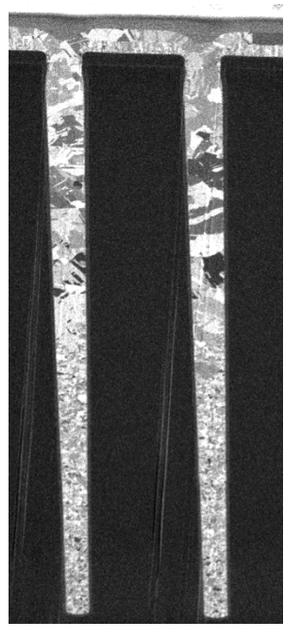
Return to
POR 5x50µm
(driven by cost reduction, ability to assemble on thin interposers & active interposer applications)

Scaling for 3D-IC applications

2012-13 →

3µm Ø,
50µm deep
AR 17:1

Ø ↘↘
AR ↗↗
Depth ≡

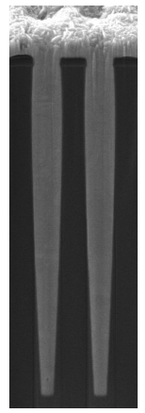


Extended scaling W2W applications

2014-16 →

2µm Ø,
30µm deep
AR 15:1

Ø ↘↘
AR ≡
Depth ↘



Minimal fill Ø ?
Max. depth ?

→ *In combination with integration on advanced device nodes*

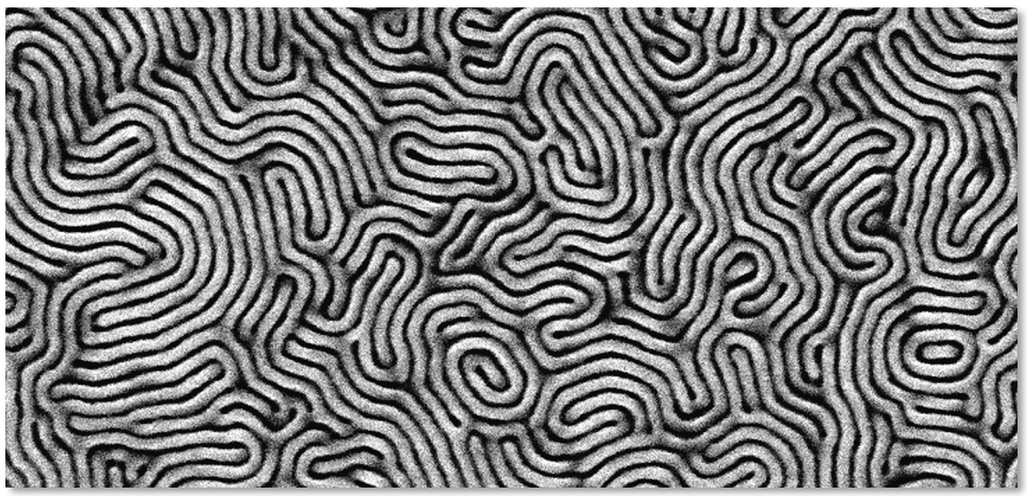
LITHOGRAPHY enabled SCALING



DIRECTED SELF ASSEMBLY

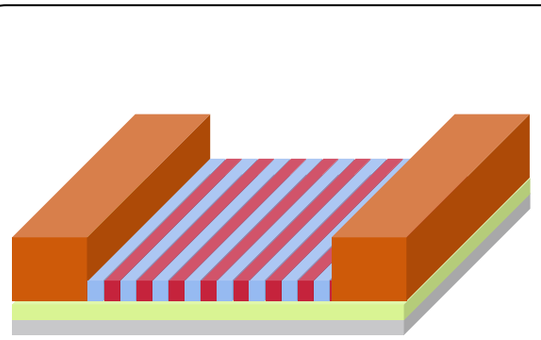
ENABLING/EXTENDING LITHOGRAPHY

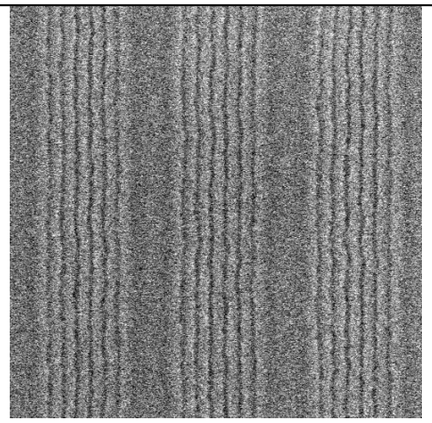
Block co-polymers (polymer constructed from 2 homo-polymers with a different polarity) can give microscopic phase separation: **self assembly**.

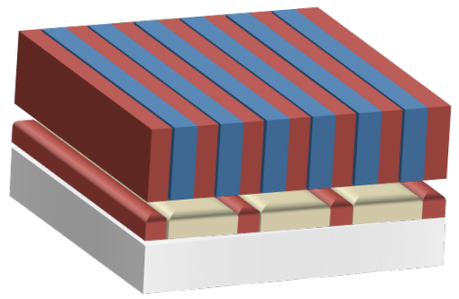


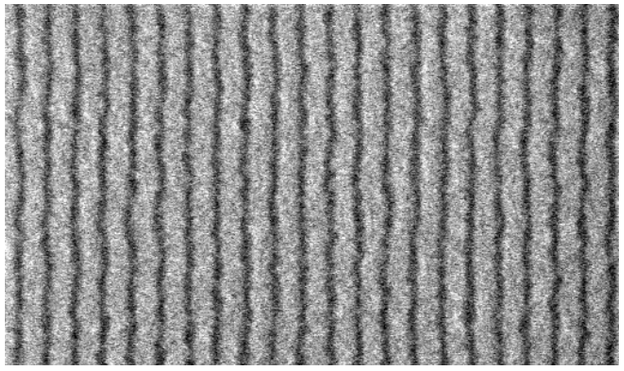


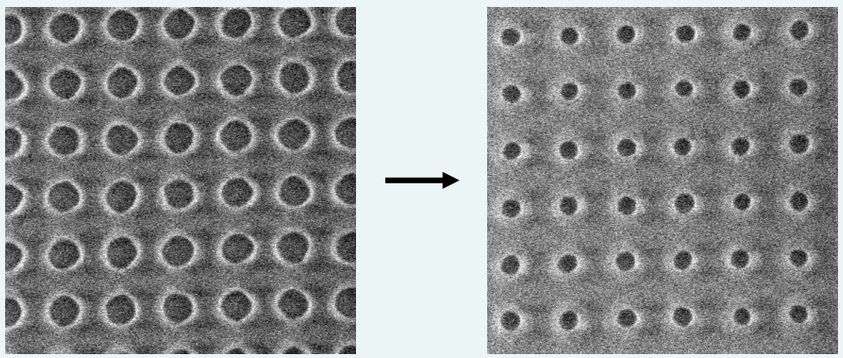
Ratio between the weights of the 2 polymers determines the 'shape'. Molecular length determines the size.

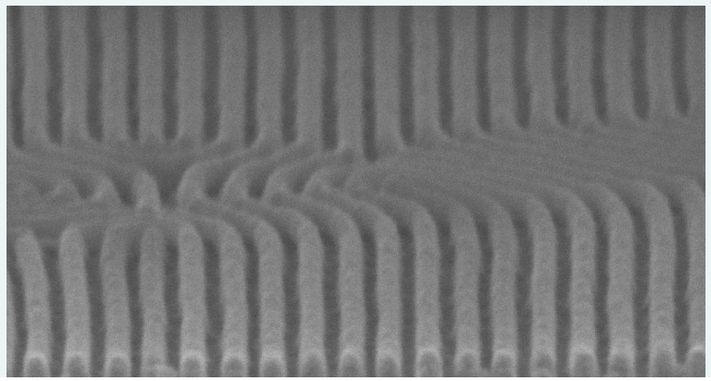






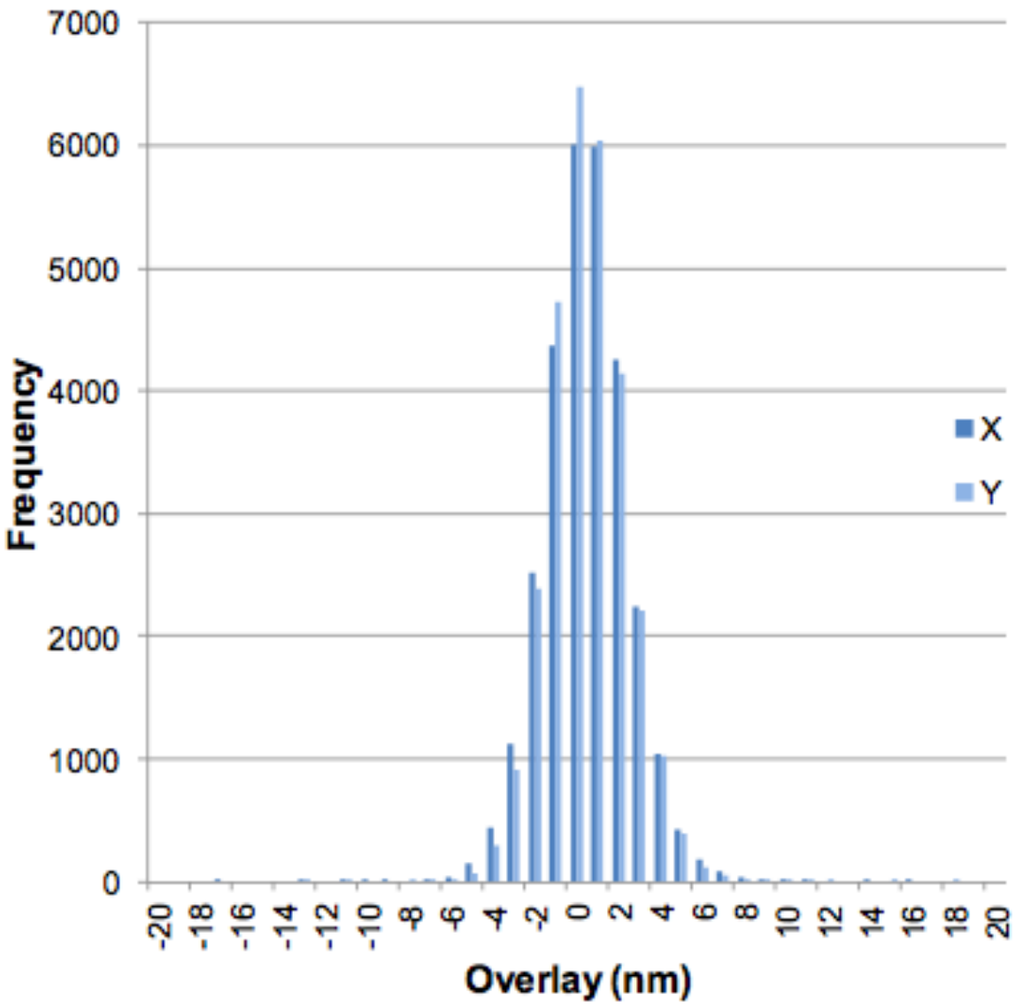




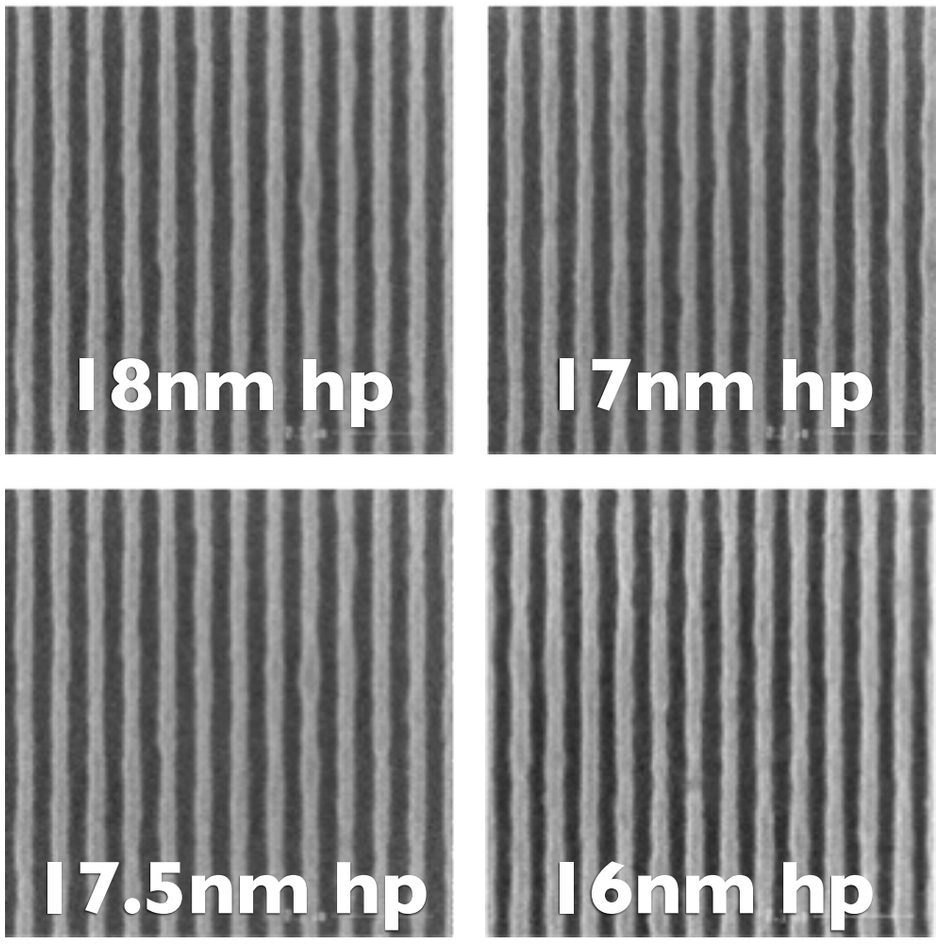


DSA shows great potential for contact hole shrink/smoothing and line multiplication.

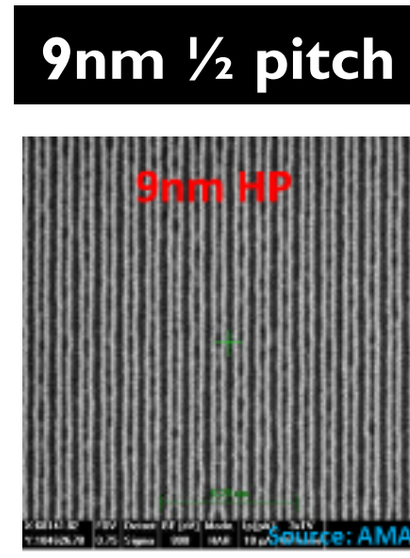
EUV LITHOGRAPHY



OVERLAY



RESOLUTION



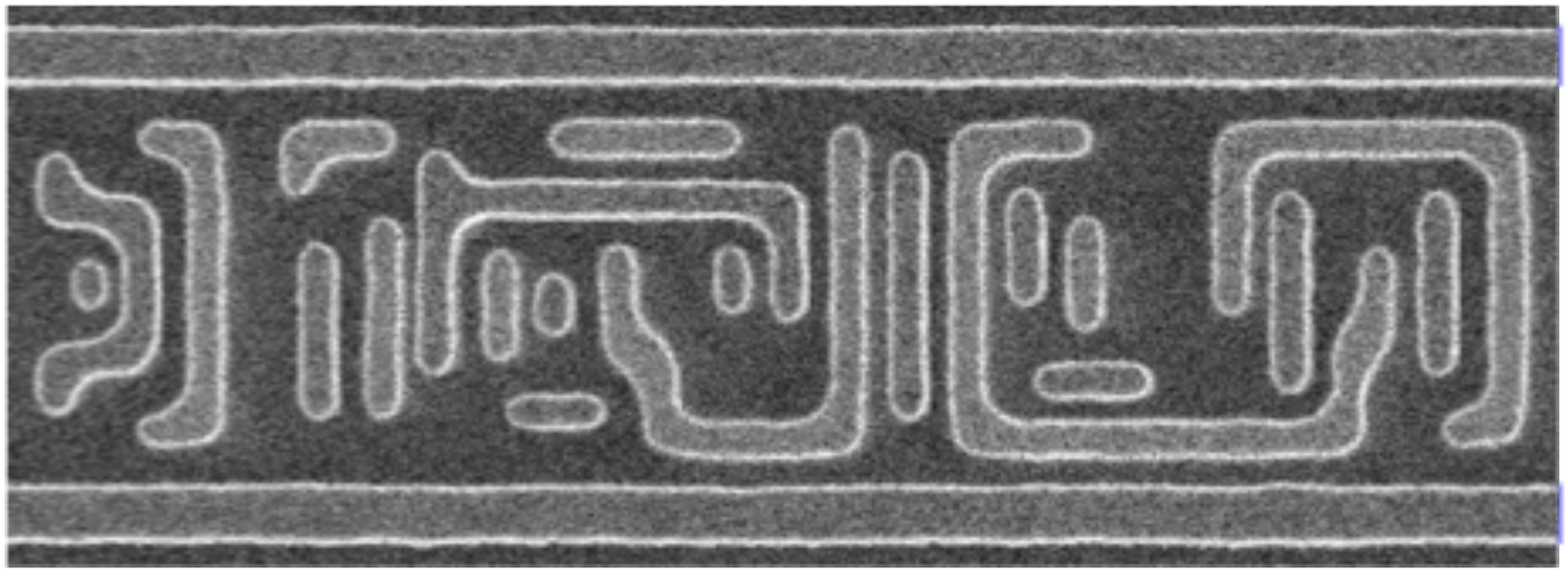
Spacer Etch

LITHOGRAPHY OPTIONS

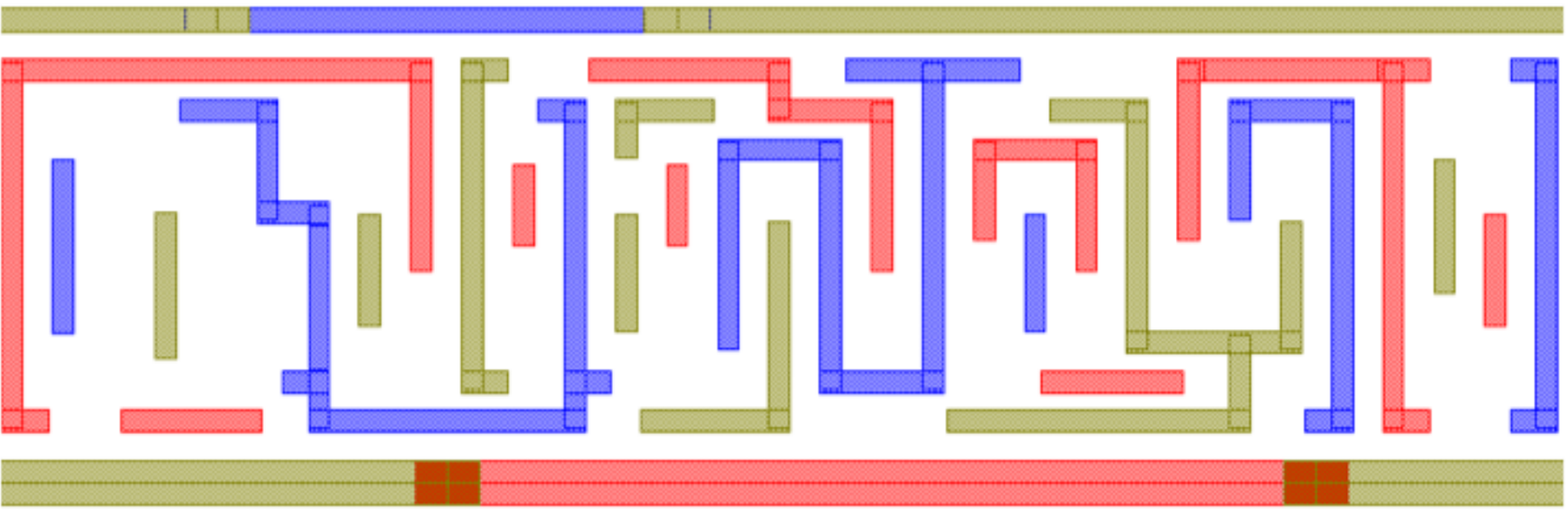
logic patterning

20 > 10nm

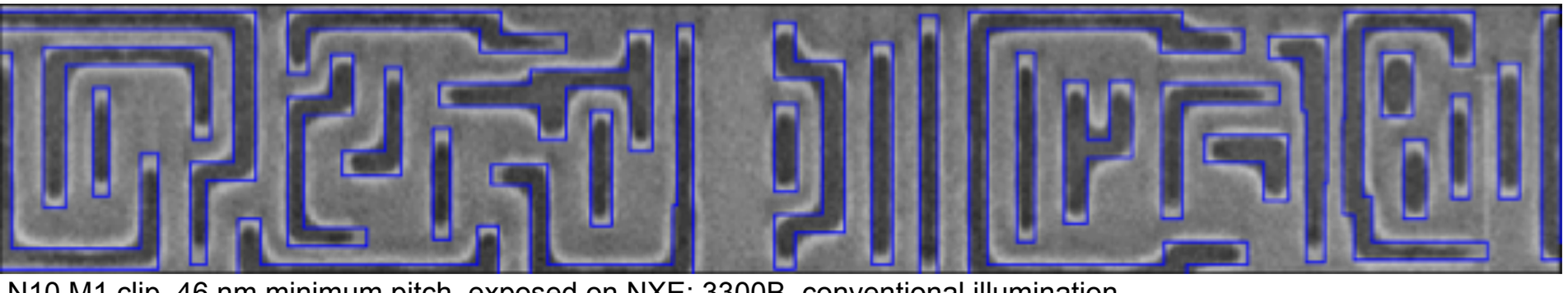
PATTERNING OPTIONS



20nm:
DP-AWARE
LAYOUT



193i TRIPLE
PATTERNING
(N10)

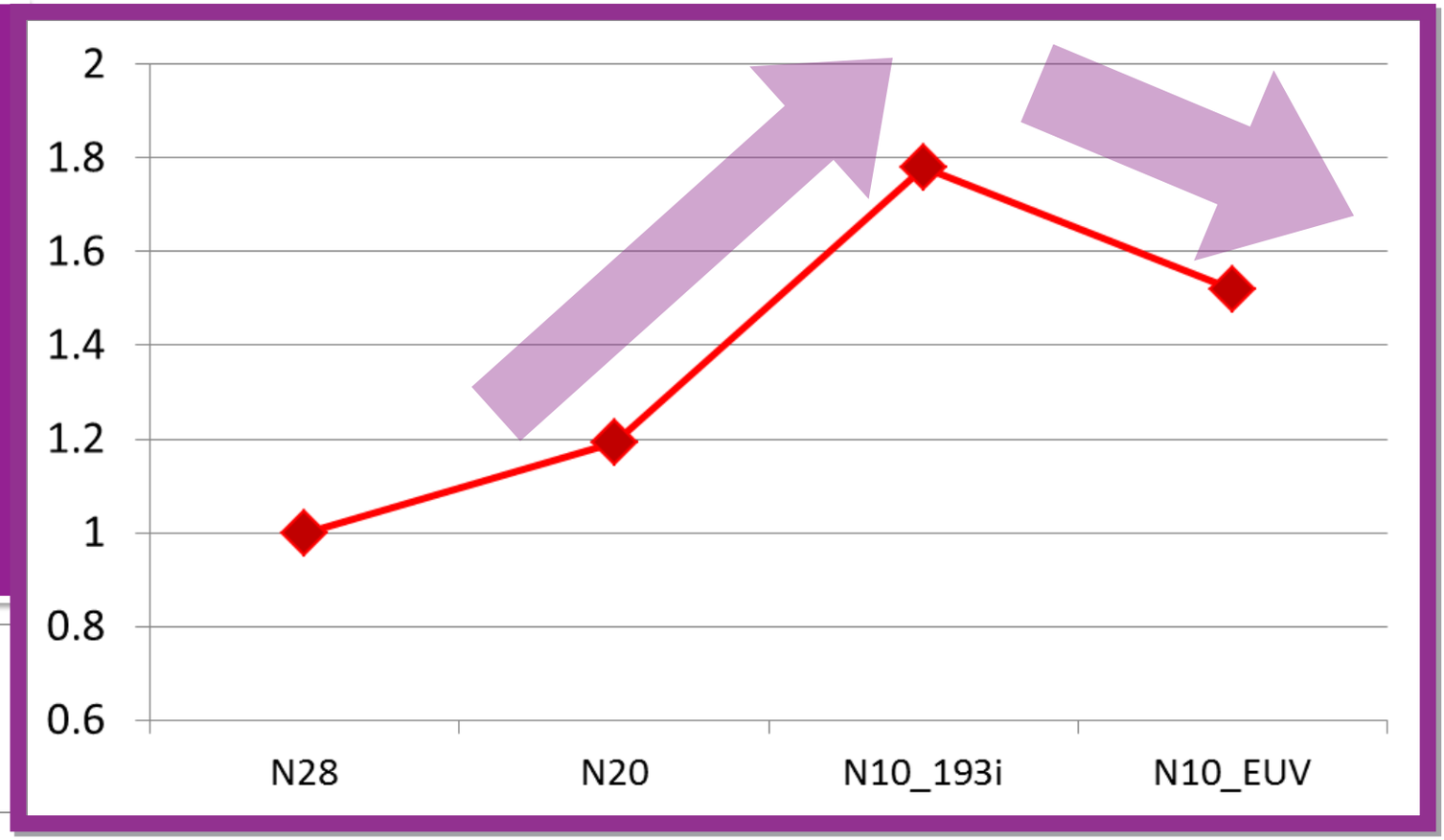


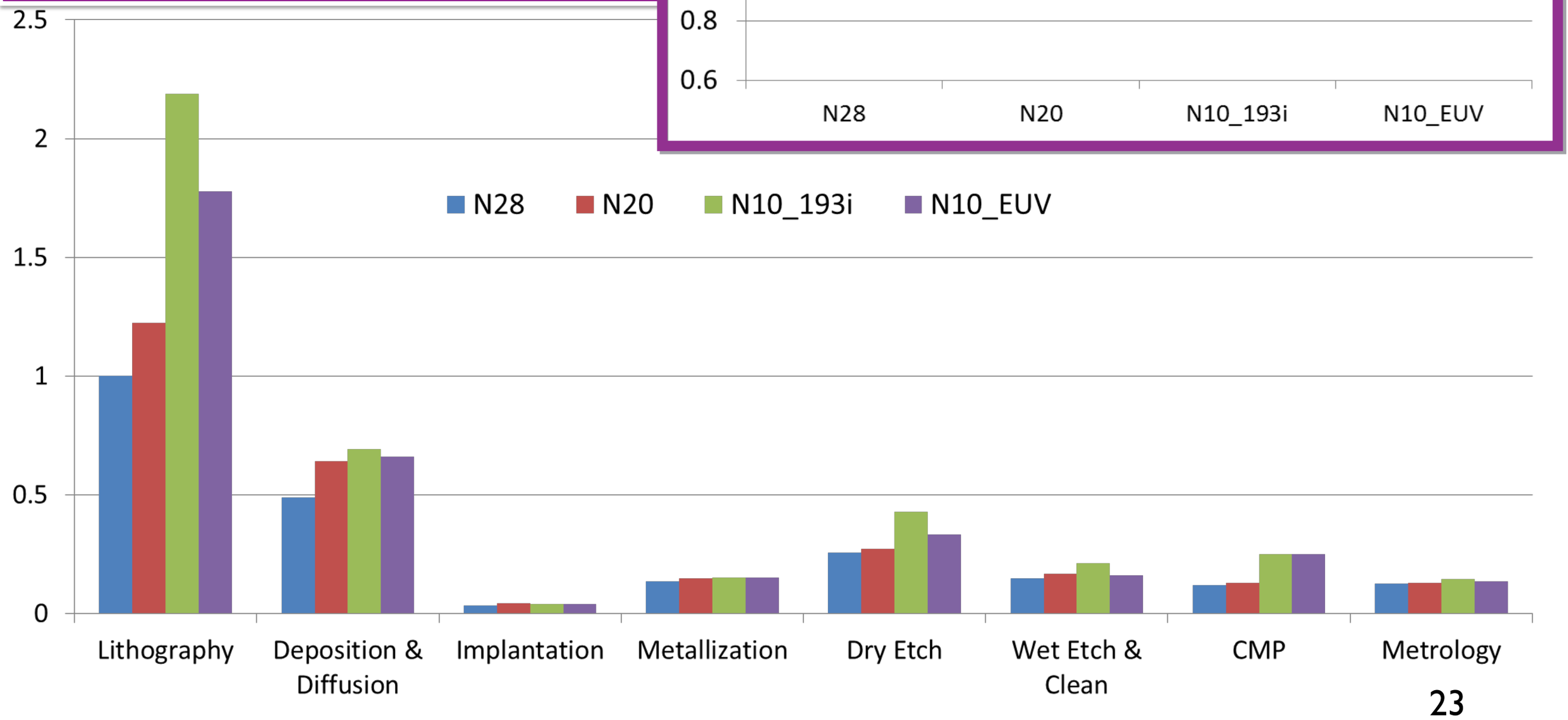
EUV 0.33 NA
SINGLE
PATTERNING

N10 M1 clip, 46 nm minimum pitch, exposed on NXE: 3300B, conventional illumination

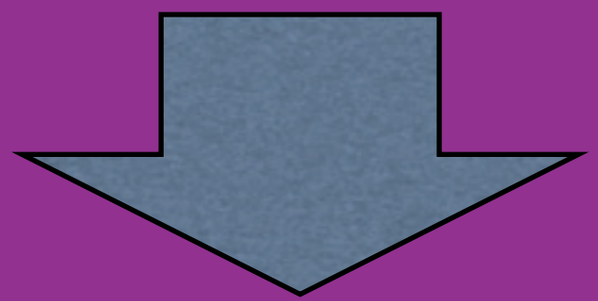
RELATIVE WAFER COST ACROSS NODES

In order to allow for cost-effective patterning steps in future technology nodes, the successful implementation of EUV as next generation lithography will be mandatory.





TECHNOLOGY GETS EXTREMELY COMPLEX



LOOKING INTO FURTHER PRODUCTIVITY IMPROVEMENT

450mm

could contribute to

cost scaling

IMEC's VIEW

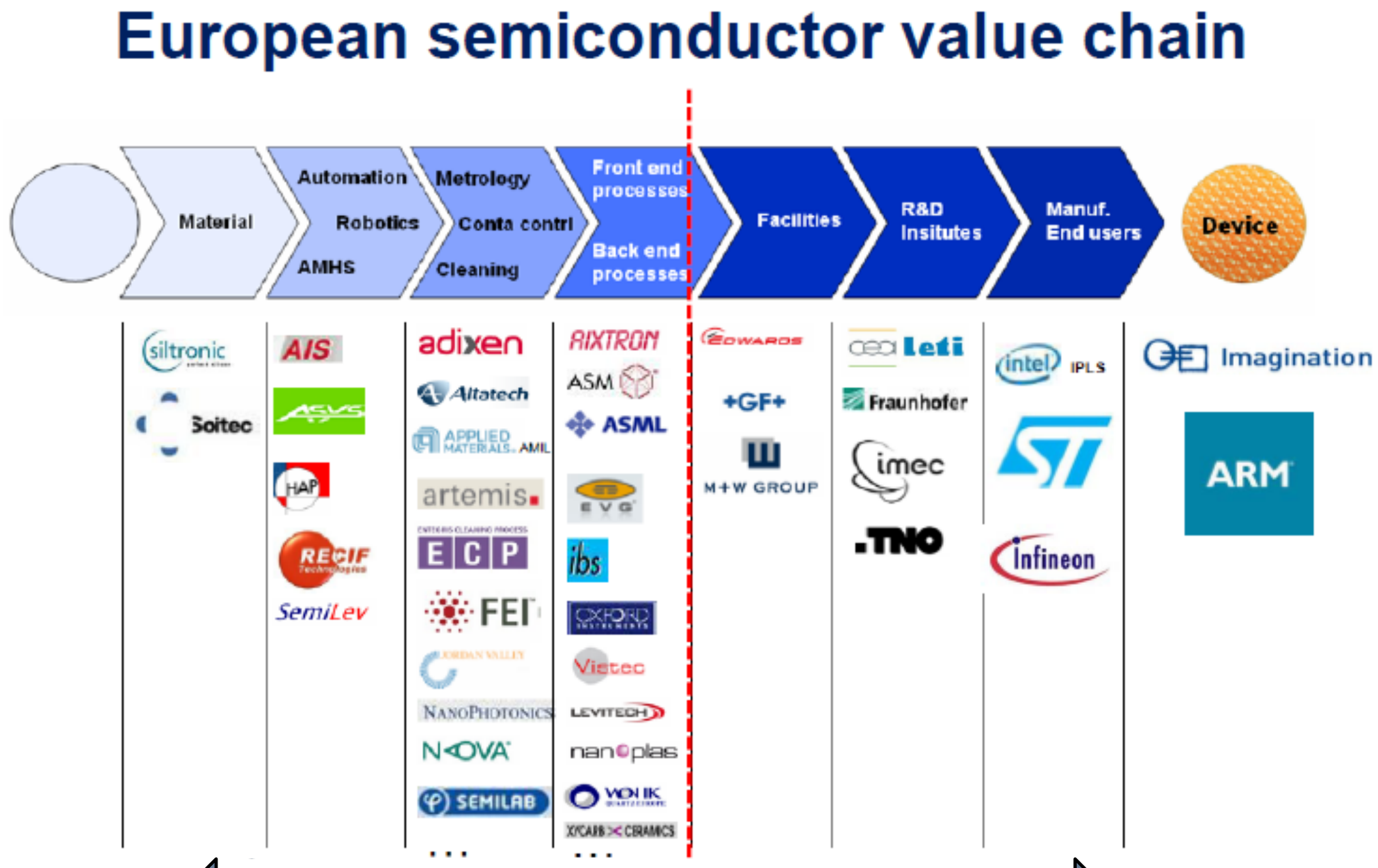
IMEC's priority is to perform leading edge process and device R&D for future nodes:

- Making EUV ready
- Screen and implement alternative device and material options; In particular high mobility materials and related process steps.
- The interconnect challenge will be addressed by material innovations, 3D stacking and optical interconnects.

Along this roadmap, somewhere in the second half of the decade, the leading industry will make the transition towards 450 mm:

- It is expected that at one point in time, the leading R&D will be done on the latest, 450mm tools.
- In order to timely address this infrastructure challenge , IMEC has launched a 450mm project, in addition to its 300mm based infrastructure, which plans to enable the process and device R&D challenges in the sub-10 nm regime.

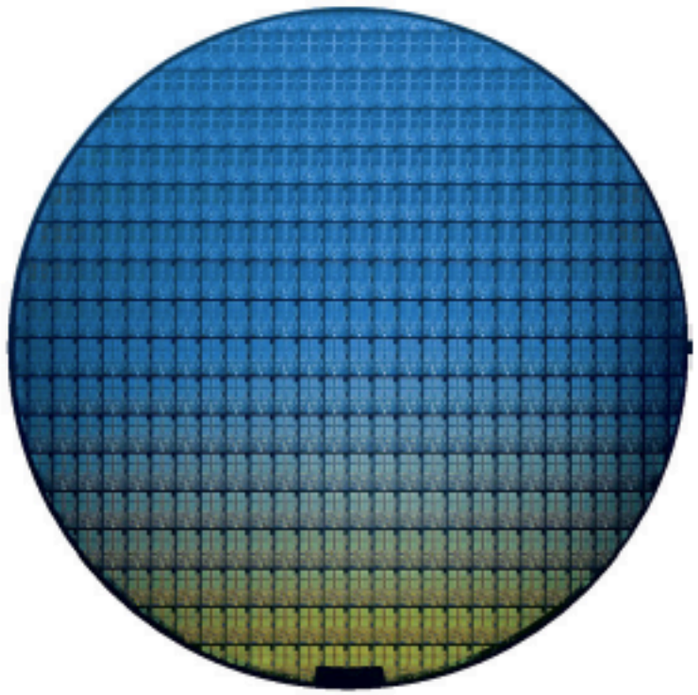
EUROPE'S ECOSYSTEM

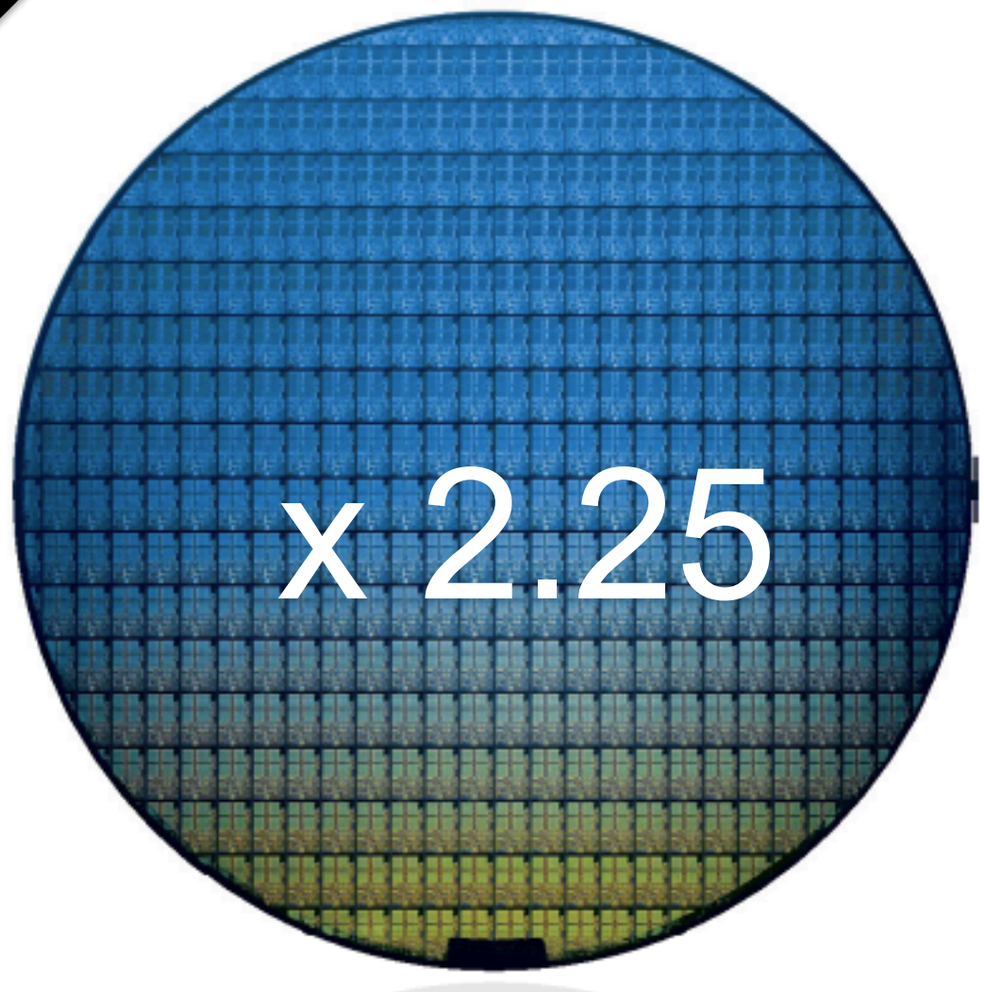


Source: ITRI/IEK Analysis; Recif

工業技術研究院 Industrial Technology Research Institute
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450mm





300 mm

450 mm

WAFER BASED PROCESSING

DEPOSITION, ETCHING, CLEANING, ...

EFFICIENCY BENEFIT:
2.25x

BODY
WAFER HANDLING
PROCESS OPTIMIZATION

(SERIAL) DIE BASED PROCESSING

LITHOGRAPHY, IMPLANT, INSPECTION, ...

EFFICIENCY BENEFIT: 1x
(2.25x reduced wph)

BODY
WAFER HANDLING
PROCESS OPTIMIZATION
THROUGHPUT

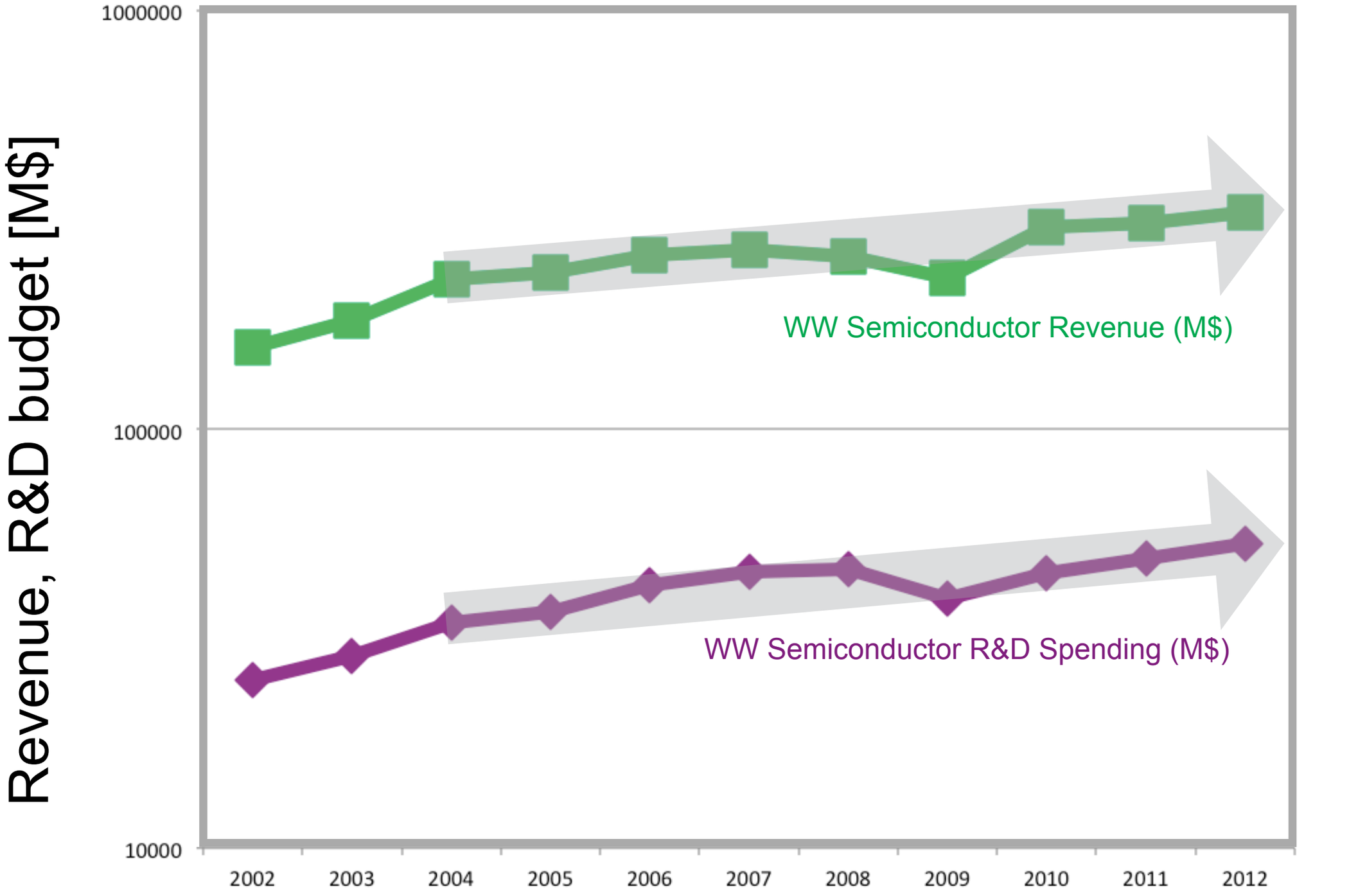
Understand

cost of ‘450’

as a measure to control

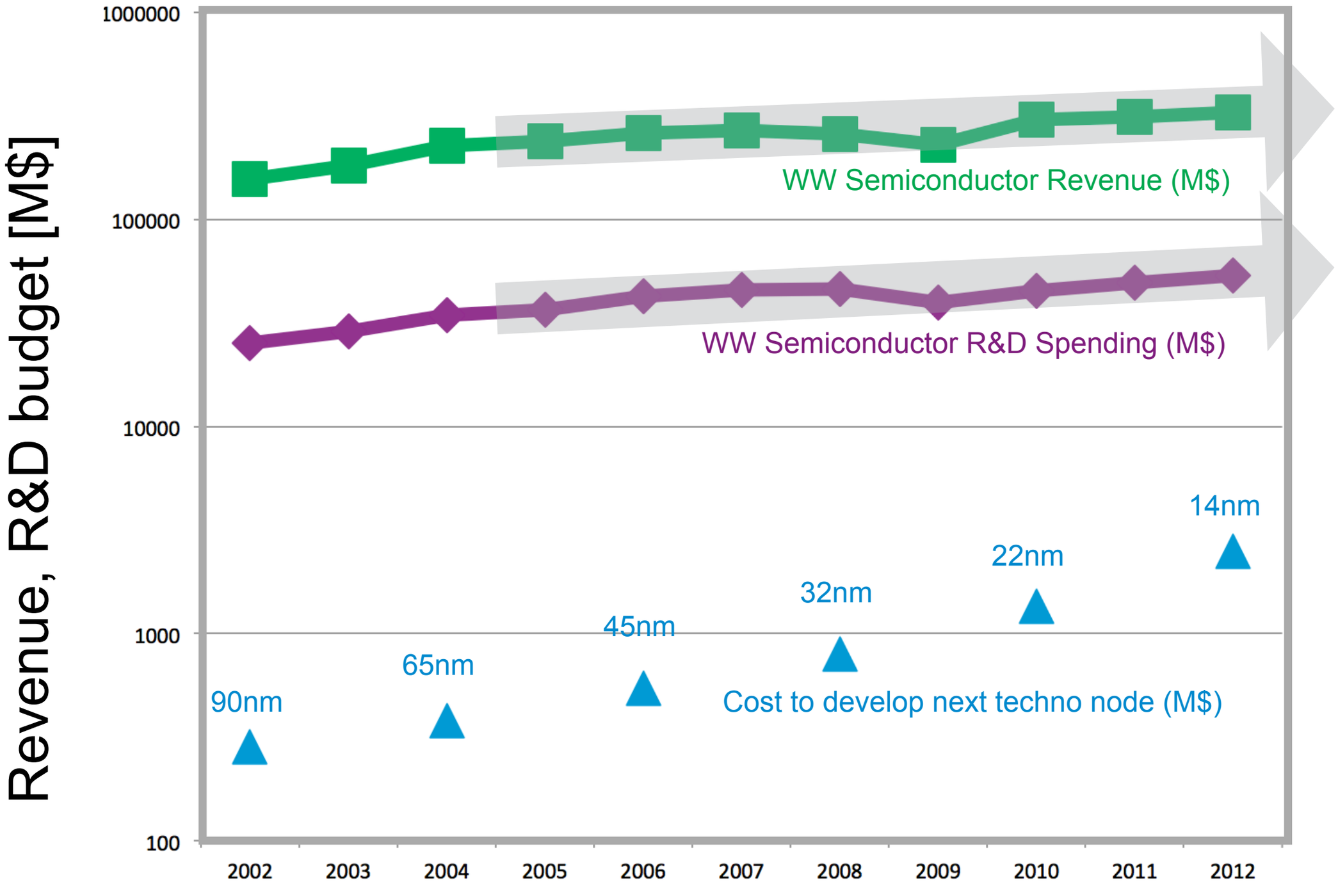
cost along the scaling roadmap

increasing R&D cost



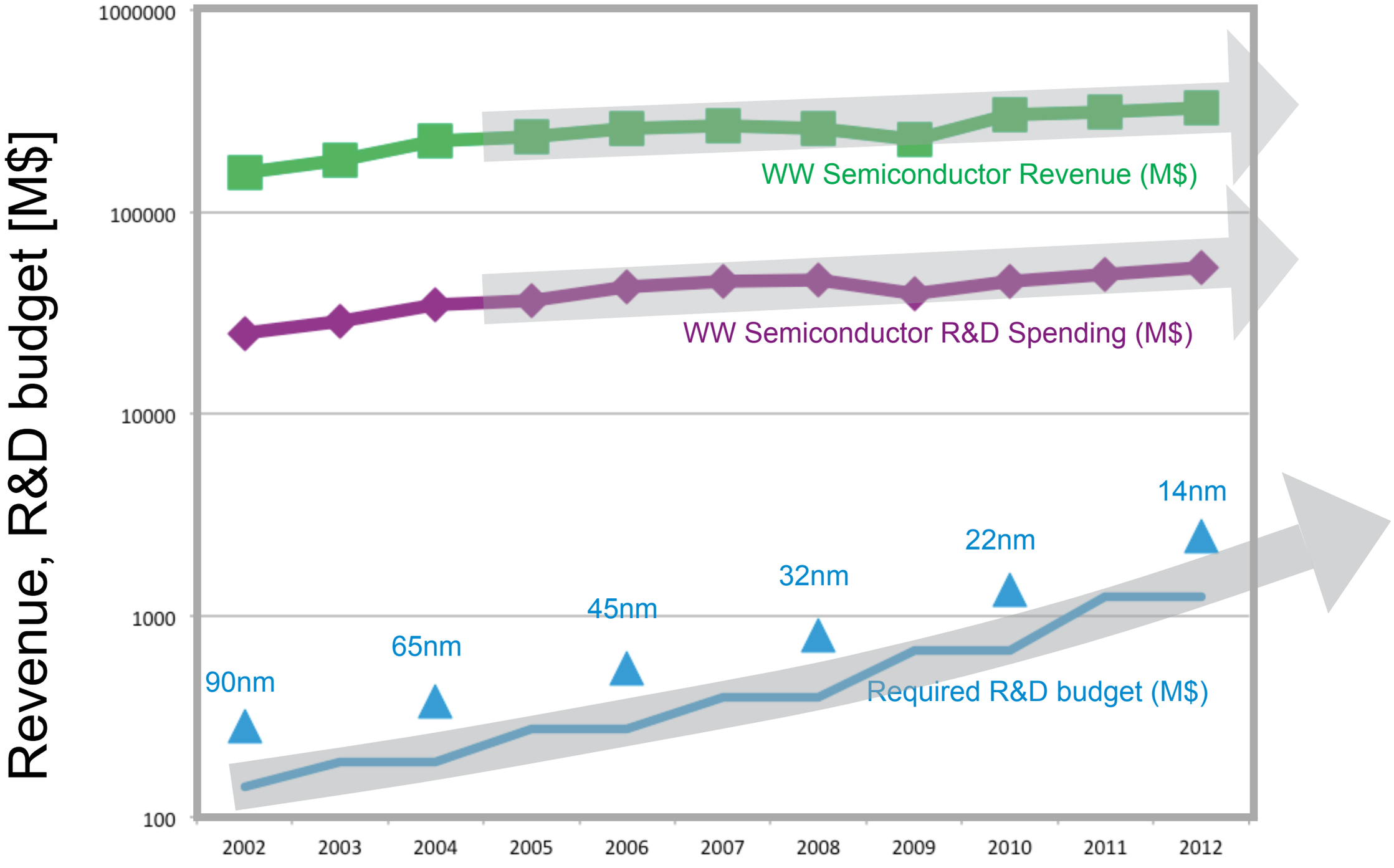
source: IHS iSupply
Sematech Report

increasing R&D cost



source: IHS iSupply
Sematech Report
IBS 2011

increasing R&D cost



source: IHS iSupply
Sematech Report
IBS 2011

NEW BUSINESS MODELS

FABLESS

FABLITE

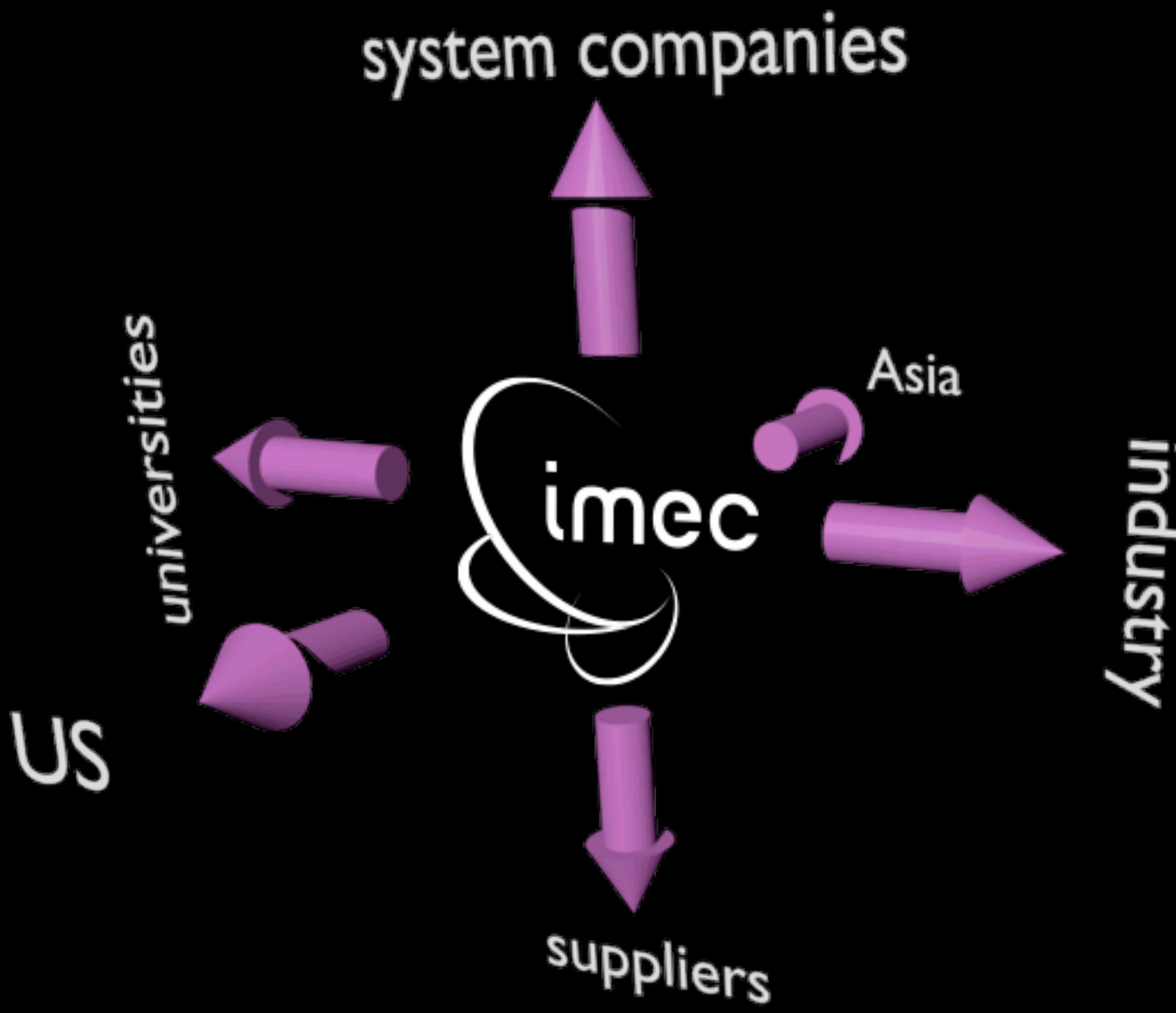
FOUND RY

OPEN INNOVATION

Collaboration

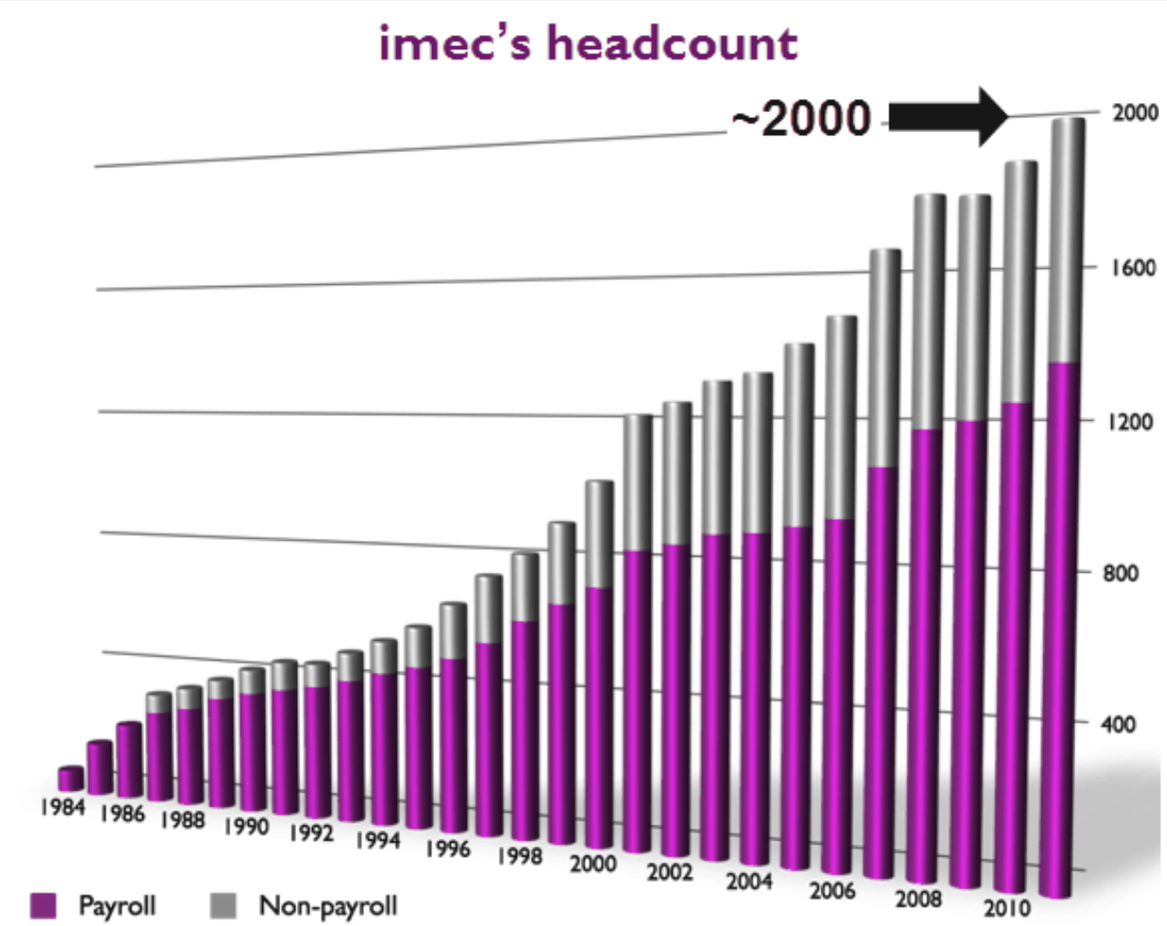
Efficient R&D

Consolidation

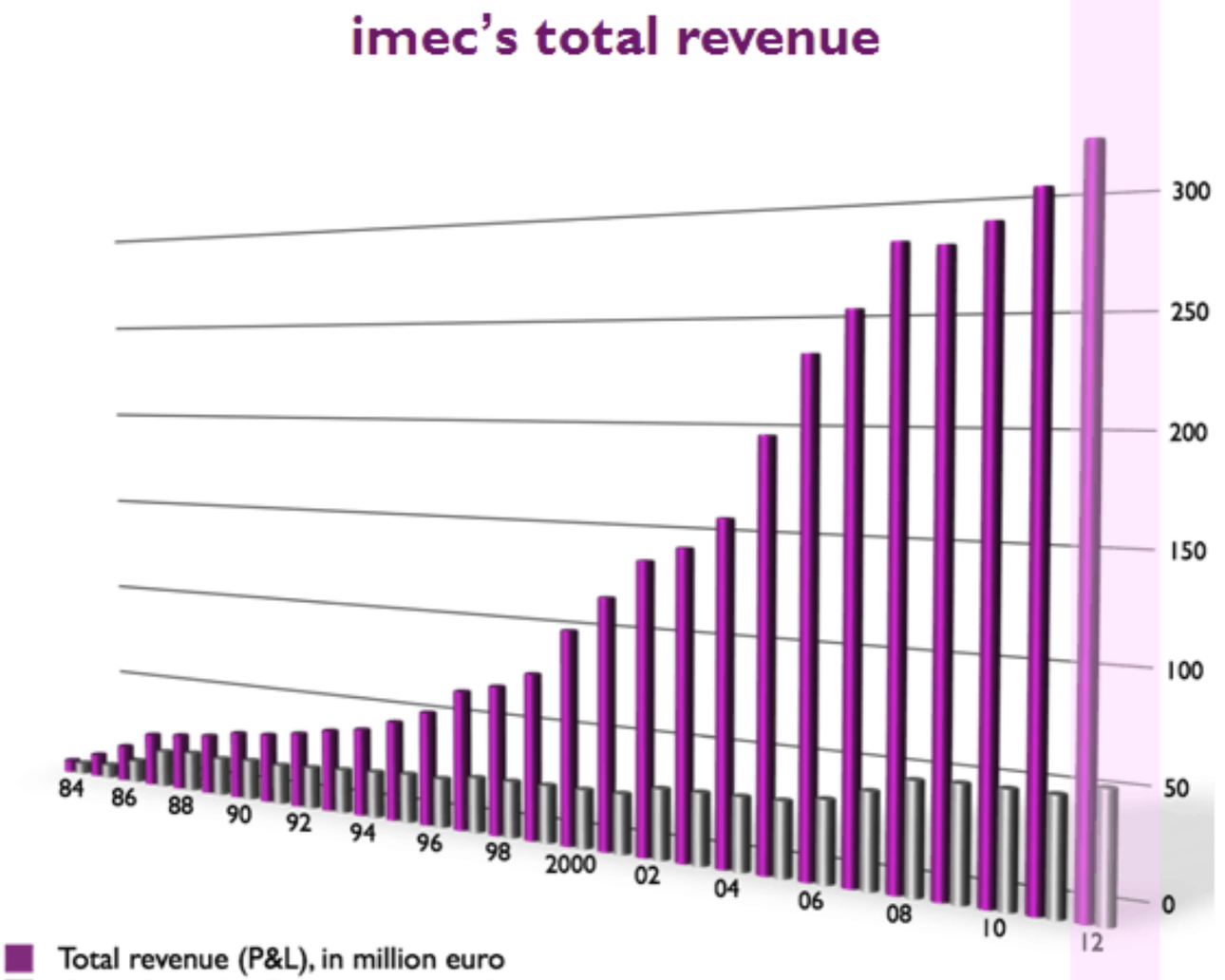

system companies
universities
Asia
US
imec
industry
suppliers

IMEC KEY DATA

imec's headcount



imec's total revenue





10000 m2 Clean Room (200mm + 300mm)
CMOS platform – n+2 technology R&D

RESEARCH PROGRAMS
FOR FULL INDUSTRY ECO SYSTEM

System Companies

SAMSUNG · Panasonic · RENESAS · HUAWEI · LG Life's Good · PHILIPS sense and simplicity · TOSHIBA Leading Innovation · Alcatel·Lucent

muRata · FUJITSU FUJITSU LABORATORIES · TARGET THE ASIP COMPANY · ALLEN INSTITUTE for BRAIN SCIENCE Fueling Discovery · HHMI HOWARD HUGHES MEDICAL INSTITUTE · wellcome trust

AVERY DENNISON · TOYOTA InfoTechnology Center Co., Ltd. · i.know · PACIFIC BIOSCIENCES · intrinsic ID · CARDIONET Get to the Heart of the Problem. · NXP founded by Philips

TOTAL · Cyberonics · NEC · soltech GDF SUEZ · kaneka · TerePac Corporation · IMS Nanofabrication · Johnson & Johnson PHARMACEUTICAL RESEARCH & DEVELOPMENT

IC Makers

Logic & Memory IDM & Foundries

intel · SAMSUNG · tsmc

TOSHIBA SanDisk · Micron · SK hynix · GLOBALFOUNDRIES

Fablite & Fabless & OSAT

Panasonic · QUALCOMM · SONY · NVIDIA · Amkor Technology · XILINX · FUJITSU · UTAC · ALTERA

Suppliers

ASML · ASM · APPLIED MATERIALS · Lam RESEARCH · KLA-Tencor · TEL ICL · SOKUDO · SUSS MicroTec · SCREEN

Mentor Graphics The EDA Technology Leader · brewer science · JSR · TOPPAN · NuFlare · SEMILAB · OXFORD INSTRUMENTS · RIXTRON · Ultratech · cadence

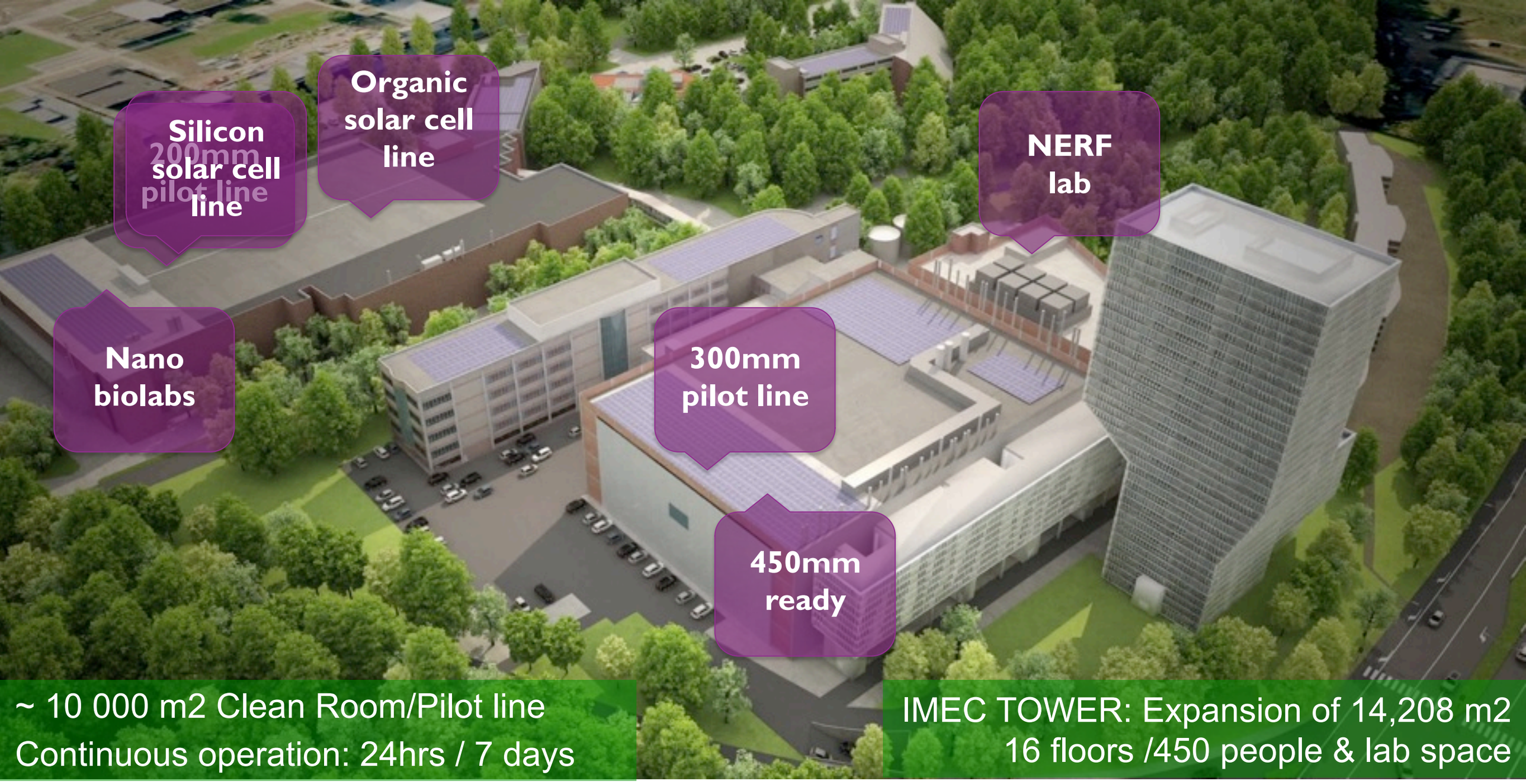
FUJIFILM · siltronic perfect silicon solutions · SunEdison simplifying solar · umicore · DNP · NISSAN Chemical America Corporation · FEI · DOW CORNING · RIBER

HITACHI Inspire the Next · SYNOPSYS Predictable Success · AZ Electronic Materials · tok · AGC · DUPONT · DISCO · BASF The Chemical Company · Entegris · ATMI

CASCADE MICROTECH · ZEISS · Soitec · Canon CANON ANELVA · JX Nippon Mining & Metals · set · DOW

Sumitomo · DONGJIN · EBARA · PVA TePla · Henkel · RENA · Hitachi Chemical Working On Wonders · Tela Innovations

ThinMaterials · EDWARDS · JORDAN VALLEY · BRUKER · Camtek · CAPRES A/S COPENHAGEN APPLIED RESEARCH



STATE-OF-THE-ART RESEARCH FACILITIES

© IMEC 2013

450mm imec TIMELINE

2012	2013	2014	2015	2016	2017	2018	2019

450mm Equipment

450mm Pilot

450mm Production

phase 1

Selected Module assessment

450mm
imec Fab1

450 mm ready facility @ imec
EEMI450, SOI450, NGC450, EEM450PR, …

Phase 2

Process & Device development in Full flow facility

450mm
imec Fab2

450 mm full flow PILOT R&D facility @ imec

450mm imec TIMELINE

2012	2013	2014	2015	2016	2017	2018	2019

450mm Equipment

MAIN FUNDING SOURCES

ENIAC
FP7

phase 1

Flemish Gov't
Industry

Selected Module assessment

450mm
imec Fab1

MAIN FUNDING SOURCES

KET
HORIZON 2020
ENIAC

Phase 2

Flemish Gov't
Industry

Process & Device development
in Full flow facility

450mm
imec Fab2

450mm Production

450 mm ready facility @ imec
EEMI450, SOI450, NGC450, EEM450PR, …

450 mm full flow PILOT R&D facility @ imec

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News & Analysis

Europe plots three pilot wafer fabs

Peter Clarke
11/21/2012 6:56 AM EST

LONDON – A European public-private partnership formed to coordinate research in nanoelectronics has proposed projects for the creation of three pilot fabs, including one for 450-mm diameter wafers. The ENIAC joint undertaking is seeking more than 800 million euro (about $1 billion) towards projects for 2012, the majority of which would be for the pilot line project proposals, according to ENIAC executive director Andreas Wild.

The ENIAC joint undertaking is a major organization set up in 2008, which brings together national funding bodies, the European

Comment

11/21/2012 8:38 PM EST
Thanks Pete! So these would be mainly state-owned facilities. The fiscal

450mm INDUSTRY TIMELINE

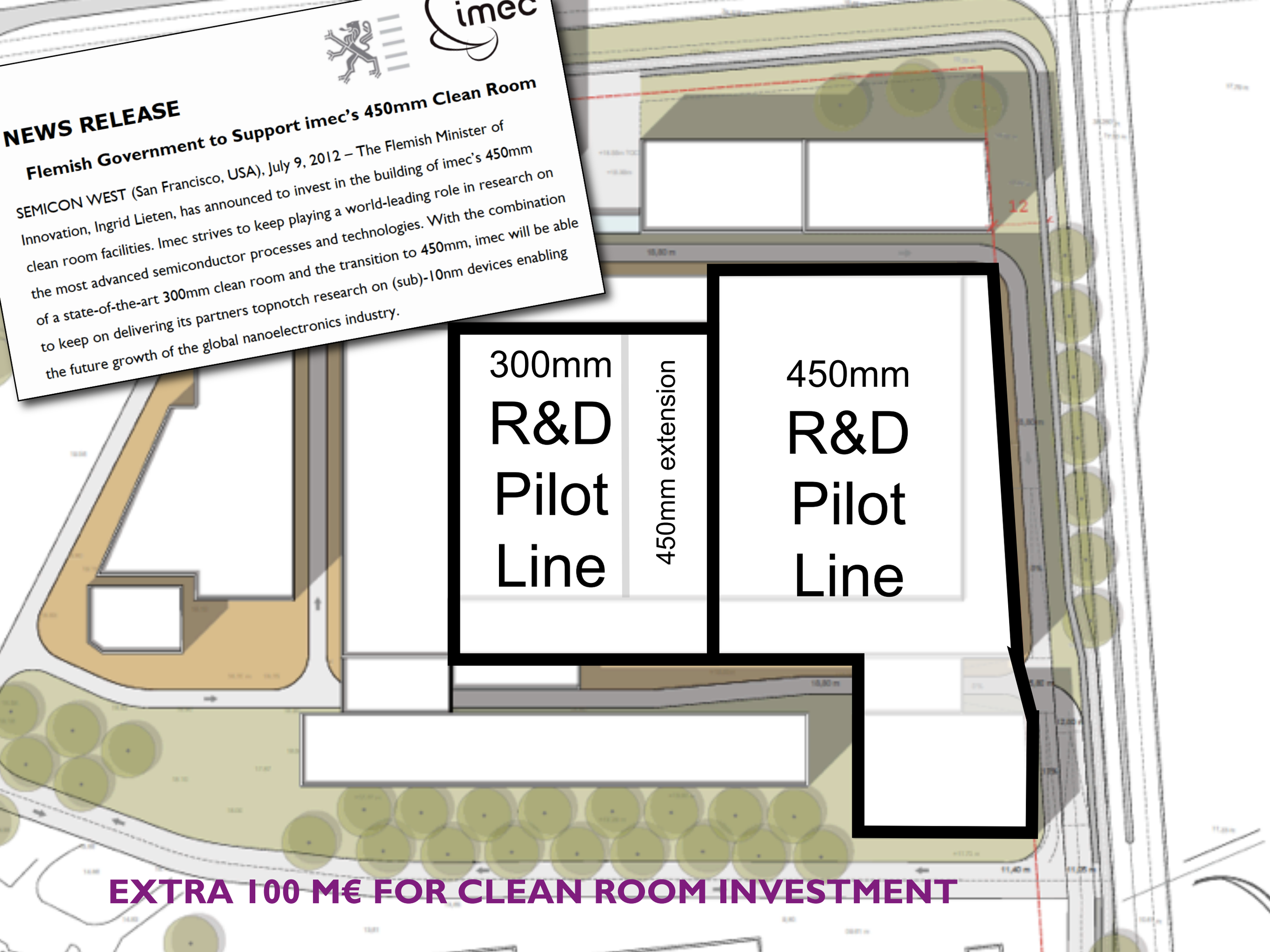
2012	2013	2014	2015	2016	2017	2018	2019

450mm Equipment

- Alpha – Hardware
- Definition of standards.
- G450C

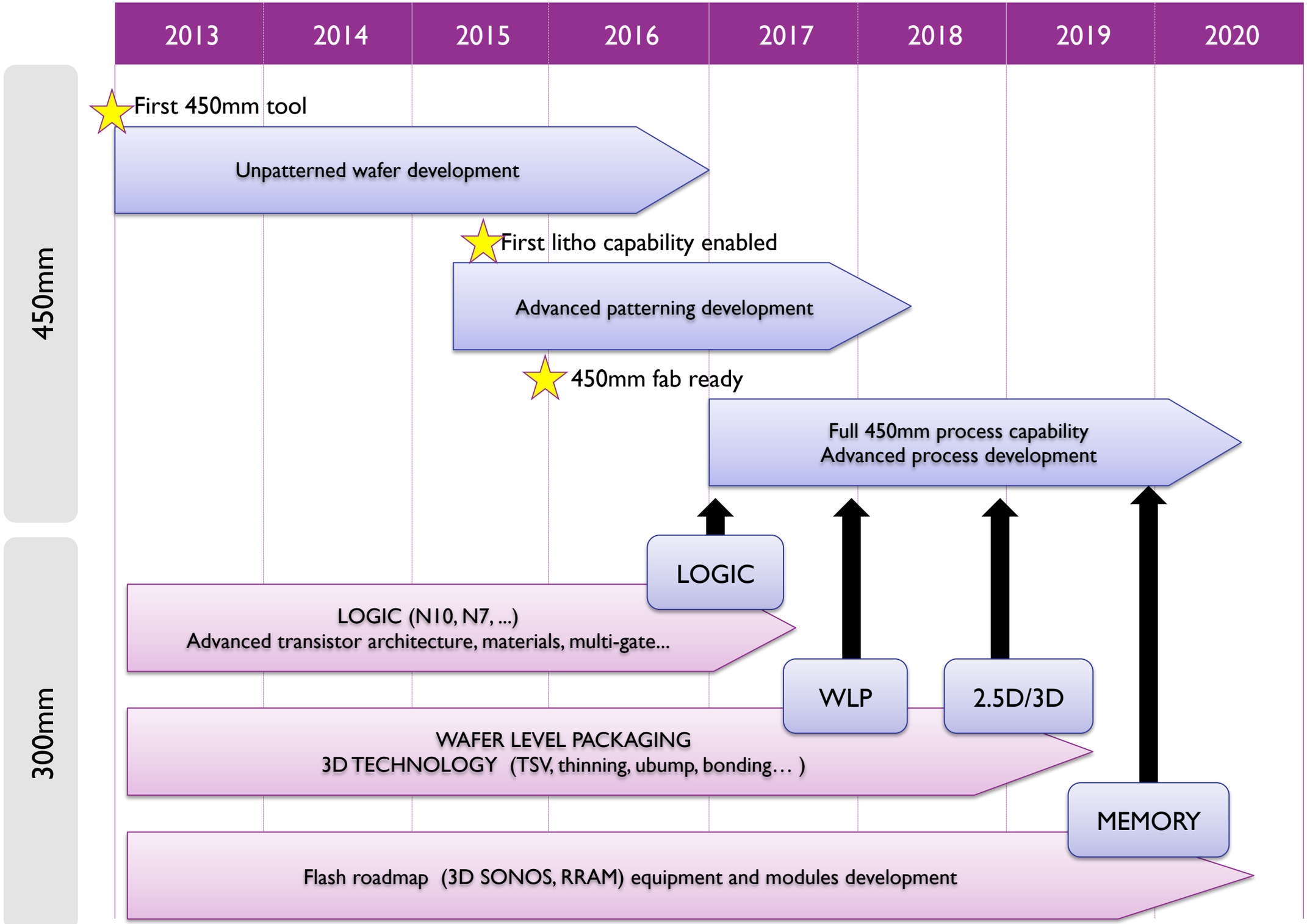
- EMI450
 EMI450PR
 EMI450EDL.




NEWS RELEASE
Flemish Government to Support imec's 450mm Clean Room
SEMICON WEST (San Francisco, USA), July 9, 2012 – The Flemish Minister of Innovation, Ingrid Lieten, has announced to invest in the building of imec's 450mm clean room facilities. Imec strives to keep playing a world-leading role in research on the most advanced semiconductor processes and technologies. With the combination of a state-of-the-art 300mm clean room and the transition to 450mm, imec will be able to keep on delivering its partners topnotch research on (sub)-10nm devices enabling the future growth of the global nanoelectronics industry.
imec
300mm
R&D
Pilot
Line
450mm extension
450mm
R&D
Pilot
Line
12
EXTRA 100 M€ FOR CLEAN ROOM INVESTMENT

450mm imec timeline

PROCESS DEVICE R&D PILOT LINE



450mm imec TIMELINE

EQUIPMENT REQUIREMENTS

Supplier roadmap perceived On-Time

Supplier roadmap perceived unclear

Supplier roadmap perceived Critical

2013 2014 2015 2016 2017 2018

300mm benchmarking

450mm wafer and film characterization

450mm scanner assessment at imec

N10 platform establishment

metrology

patterning

process tools

1 2 3 4 5 6 7 8

IMEC's CMOS PROGRAM RATIONALE

ROADMAP CHALLENGES:

- COST INCREASE
- MULTITUDE OF MATERIALS & CONCEPTS
- COMPLEXITY INCREASE



NARROWING DOWN OPTIONS,
COST SHARING & RISK MITIGATION ARE KEY

The ConFab®

Thank You!

imec